8-Output, 8-bit PWM LED Driver with Supply Regulation Feedback

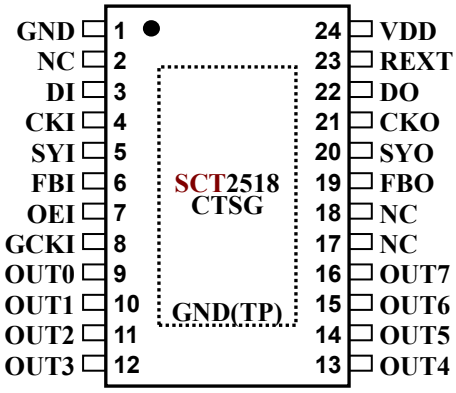
Product Description

The SCT2518 is a patented SPI+™ interface design for simplicity of backlight local dimming control. It's an 8-bit constant current sink driver incorporating shift registers and data latches for SPI interface. When the dimming data bytes are written into the SCT2518 in sequence, the patented design initiates a new PWM dimming signal for the output as soon as its luminance data is updated. The maximum current value of all 8 outputs is determined by an external resistor and is adjustable with the OEI signal. Each output also has individual 8-bit PWM dimming control. The SCT2518 provides patented logical feedback to automatically regulate the LED supply voltage and hence minimizes the system power consumption.

Features

- Patented SPI+™ interface for simplicity of local dimming control
- Patented logical feedback for automatic supply regulation
- LED brightness local dimming and scanning mode control are supported
- High linearity gray response with accurate 1 to 100% PWM dimming control
- Real-time dot correction of luminance
- Backlight local dimming controller available
- Built-in internal PWM clock, 8 independent 8-bit PWM digital current controlled outputs
- Vsync frame start and external PWM clock input for Hsync synchronization are available
- Power-on open detection to bypass unconnected or broken LED strings
- 8 constant current sinkers with output voltage sustainable to 24V
- Excellent regulation to load, supply voltage and temperature
  Temperature regulation: ±0.005%/°C, load regulation: ±0.1%/V, line regulation: ±0.5%/V
- High current matching accuracy: ±1% between outputs, ±2% between ICs
- Constant output current : 20 – 90/120mA@3.3/5V
- Low dropout voltage 0.8V@120mA, V_{DD}=5V
- Output current is set by a single external resistor and OEI programmable outputs
- Buffered outputs to regenerate input signals for cascaded operation
- CMOS Schmitt trigger inputs
- Built-in power on reset(POR) circuit forces all the outputs ON while power on
- Built-in thermal protection function to prevent damage from over current operation
- Package: TSSOP24 with thermal pad
- Applications: Local dimming LED backlight

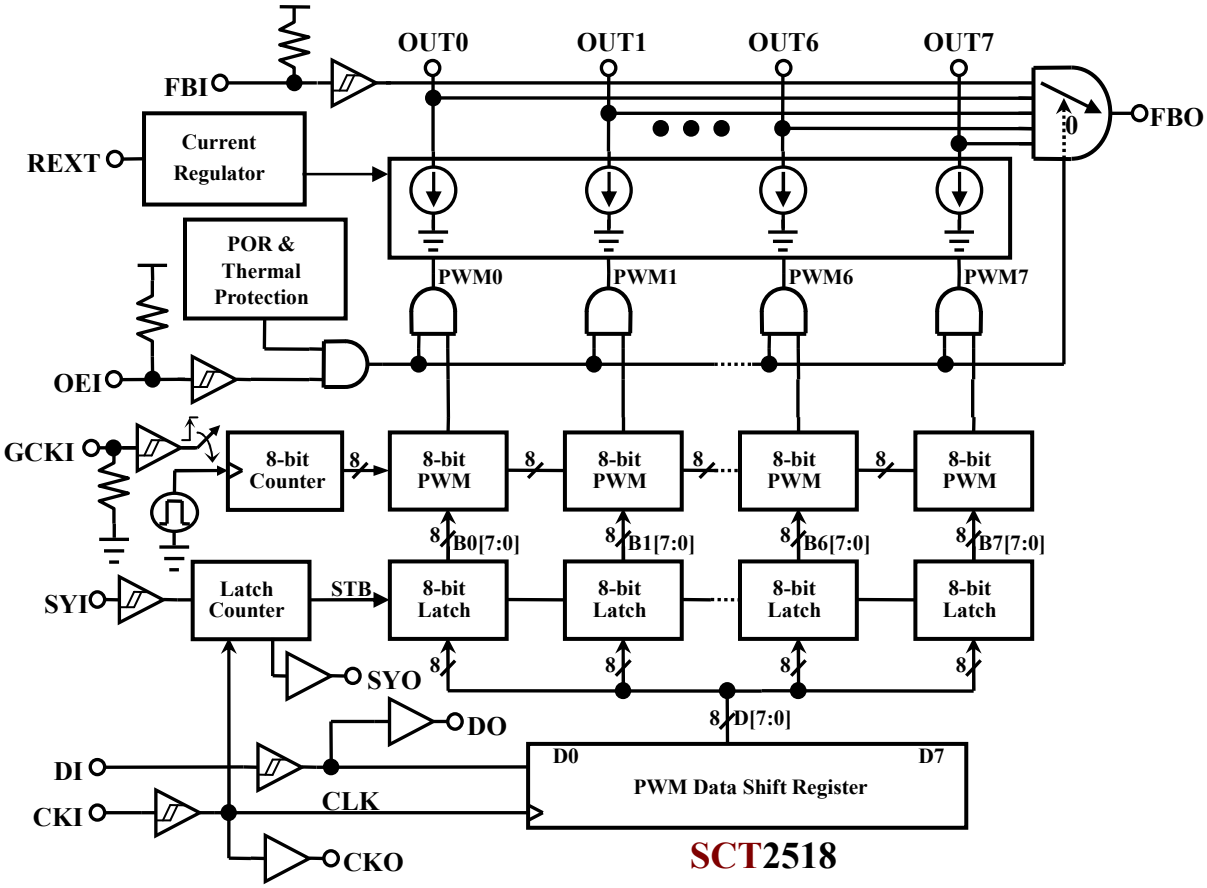
Pin Configurations



Terminal Description

Pin Name	Pin No.	I/O	Function
GND	1	-	Ground terminal
NC	2	-	No connection
DI	3	I	Serial input of data shift register.
CKI	4	I	Clock input of shift register with data sampled at the rising edge of CKI.
SYI	5	I	Synchronous signal, daisy chain input terminal. When power on, the default status of SYI is low. Only the rising edge of SYI causes the SCT2518 begin to latch data byte form 8-bit shift register.
FBI	6	I	Logical feedback input, comes from FBO of another SCT2518. During the power on open detection process, user may add proper RC to detect the open LED strings.
OEI	7	I	Global brightness control input. All outputs are enabled when OEI is high. When OEI is high, all outputs are turned on or off by their PWM data that starts the built-in 8-bit PWM function. When OEI is low, all outputs are disabled. The internal enable signal synchronizes to PWM clock automatically and therefore be advised to set OEI pulse width larger than PWMCLK period.
GCKI	8	I	External global clock input for PWM operation. The internal PWM clock is automatically switched to GCLK if this pin is applied with external clock. By default, the built-in oscillator is employed for PWM operation.
OUT[0:7]	9-16	O	Open-drain, constant-current outputs.
NC	17-18	-	No connection
FBO	19	O	Logical feedback output. FBO is low when ANY of OUT is less than 1V, FBO is high when ALL of OUTs are greater than 1V. When OEI = ”0” FBO will reflect the FBI input, thus the previous FBO information can be carried to next IC.
SYO	20	O	Synchronous signal, daisy chain output terminal.
CKO	21	O	Buffered output of CKI
DO	22	O	Buffered output of DI
REXT	23	I/O	Used to connect an external resistor for setting up all output current
VDD	24	-	Supply voltage terminal
GND	TP	-	Thermal pad, as ground terminal of open-drain output

Block Diagram

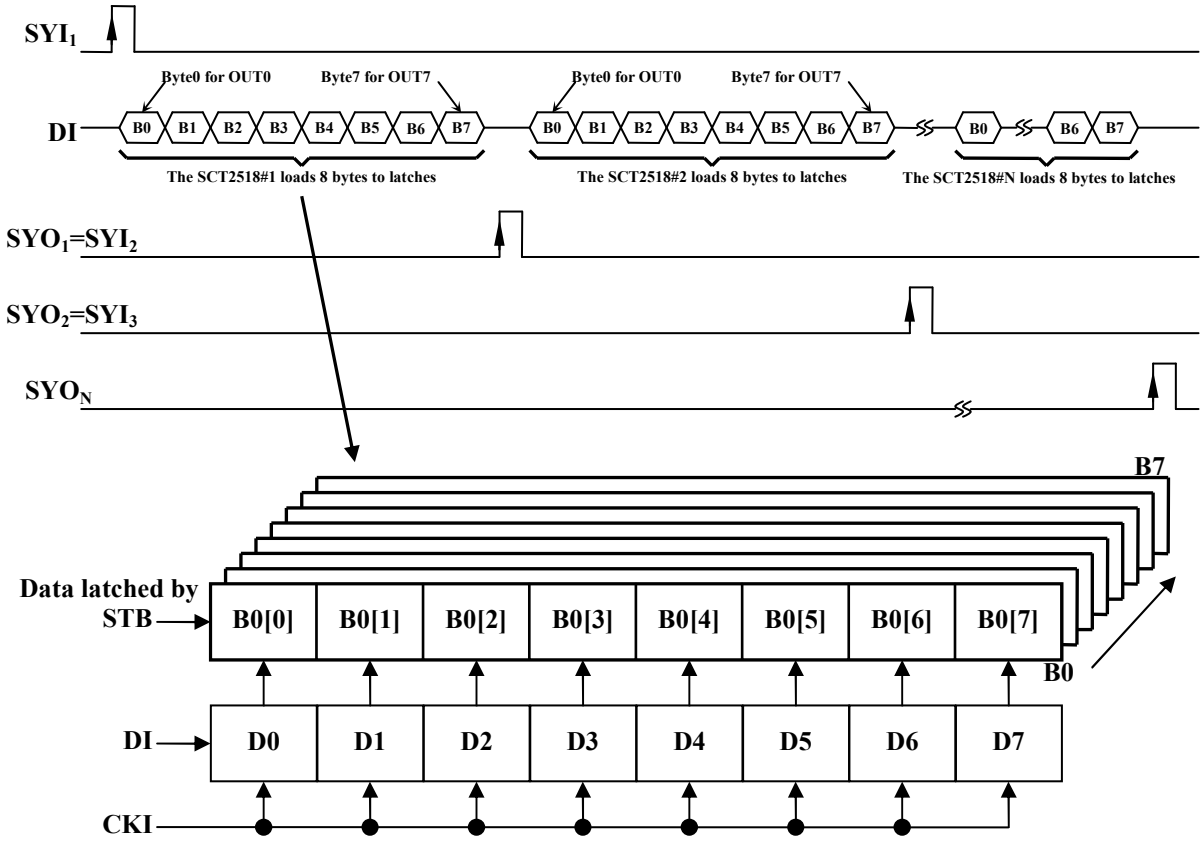


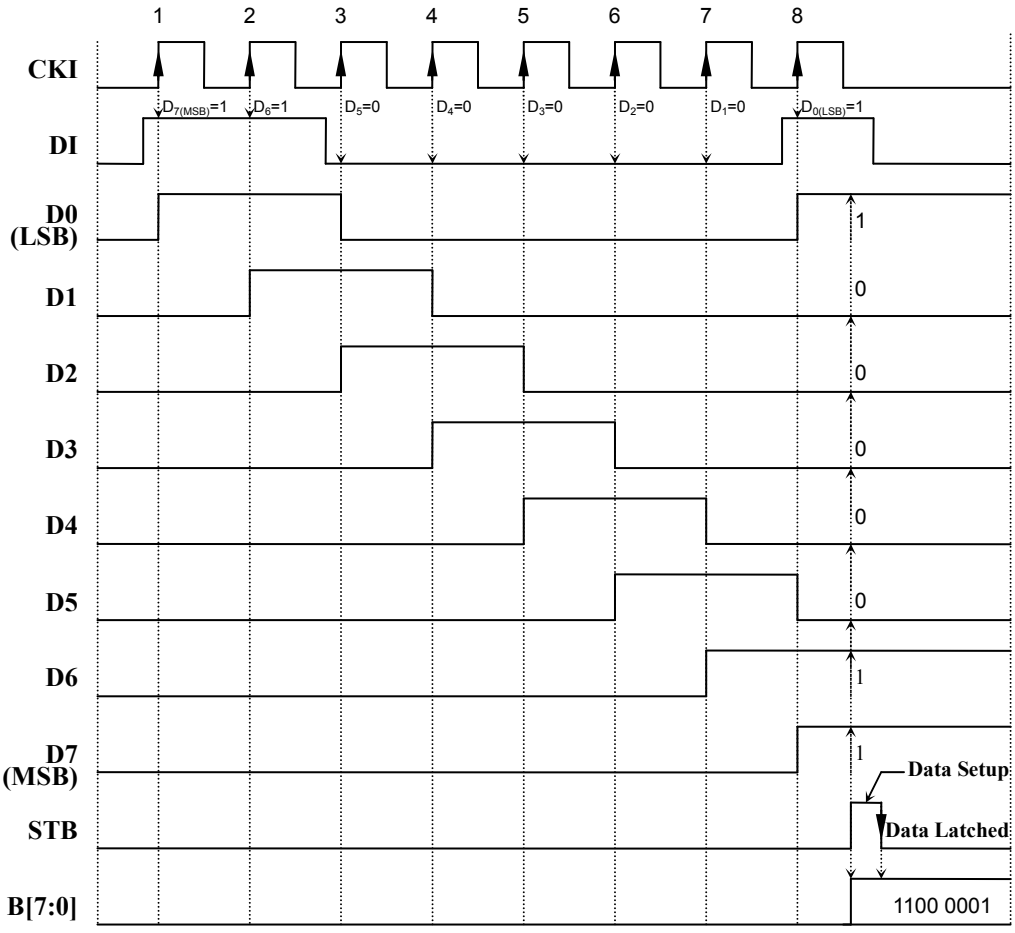
Truth Table

CKI	DI		D[0:7] of Register	B0[7:0]	B1[7:0]	B2[7:0]	B3[7:0]	..B7[7:0]
8*↑	D_{0X}	$D_{07\text{-}00}$	$D_{00}D_{01}D_{02}D_{03}D_{04}D_{05}D_{06}D_{07}$	$D_{07\text{-}00}$	NC	NC	NC	NC
↑	D_{1X}	D_{17}	$D_{17}D_{00}D_{01}D_{02}D_{03}D_{04}D_{05}D_{06}$	NC*	NC	NC	NC	NC
↑		D_{16}	$D_{16}D_{17}D_{00}D_{01}D_{02}D_{03}D_{04}D_{05}$	NC	NC	NC	NC	NC
↑		D_{15}	$D_{15}D_{16}D_{17}D_{00}D_{01}D_{02}D_{03}D_{04}$	NC	NC	NC	NC	NC
↑		D_{14}	$D_{14}D_{15}D_{16}D_{17}D_{00}D_{01}D_{02}D_{03}$	NC	NC	NC	NC	NC
↑		D_{13}	$D_{13}D_{14}D_{15}D_{16}D_{17}D_{00}D_{01}D_{02}$	NC	NC	NC	NC	NC
↑		D_{12}	$D_{12}D_{13}D_{14}D_{15}D_{16}D_{17}D_{00}D_{01}$	NC	NC	NC	NC	NC
↑		D_{11}	$D_{11}D_{12}D_{13}D_{14}D_{15}D_{16}D_{17}D_{00}$	NC	NC	NC	NC	NC
↑		D_{10}	$D_{10}D_{11}D_{12}D_{13}D_{14}D_{15}D_{16}D_{17}$	NC	$D_{17\text{-}10}$	NC	NC	NC
↑	D_{2X}	D_{27}	$D_{27}D_{10}D_{11}D_{12}D_{13}D_{14}D_{15}D_{16}$	NC	NC	NC	NC	NC
↑		D_{26}	$D_{26}D_{27}D_{10}D_{11}D_{12}D_{13}D_{14}D_{15}$	NC	NC	NC	NC	NC
↑		D_{25}	$D_{25}D_{26}D_{27}D_{10}D_{11}D_{12}D_{13}D_{14}$	NC	NC	NC	NC	NC
↑		D_{24}	$D_{24}D_{25}D_{26}D_{27}D_{10}D_{11}D_{12}D_{13}$	NC	NC	NC	NC	NC
↑		D_{23}	$D_{23}D_{24}D_{25}D_{26}D_{27}D_{10}D_{11}D_{12}$	NC	NC	NC	NC	NC
↑		D_{22}	$D_{22}D_{23}D_{24}D_{25}D_{26}D_{27}D_{10}D_{11}$	NC	NC	NC	NC	NC
↑		D_{21}	$D_{21}D_{22}D_{23}D_{24}D_{25}D_{26}D_{27}D_{00}$	NC	NC	NC	NC	NC
↑		D_{20}	$D_{20}D_{21}D_{22}D_{23}D_{24}D_{25}D_{26}D_{27}$	NC	NC	$D_{27\text{-}20}$	NC	NC
8*↑	D_{3X}	$D_{37\text{-}30}$	$D_{30}D_{31}D_{32}D_{33}D_{34}D_{35}D_{36}D_{26}$	NC	NC	NC	$D_{37\text{-}30}$	NC
..8*↑	..D_{7X}	..$D_{77\text{-}70}$	$D_{70}D_{71}D_{72}D_{73}D_{74}D_{75}D_{76}D_{77}$	NC	NC	NC	NC	$D_{77\text{-}70}$
↓	D_X		$D_{70}D_{71}D_{72}D_{73}D_{74}D_{75}D_{76}D_{77}$	NC	NC	NC	NC	NC

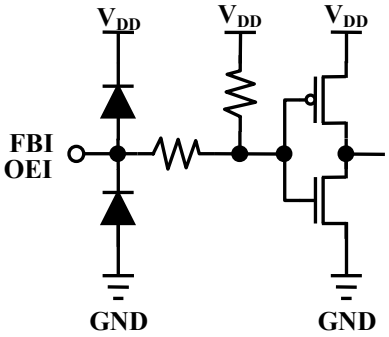
*NC: No Change, D_{1X} e.g D_{17}/D_{10} means the MSB/LSB of byte1 data.

Timing Diagram

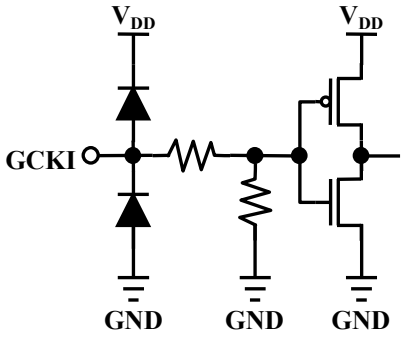




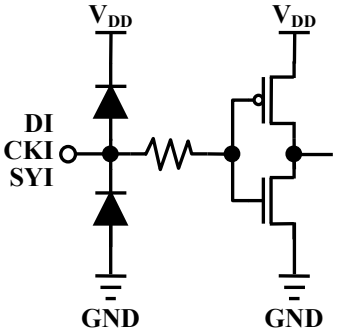
Equivalent Circuits of Inputs (1)



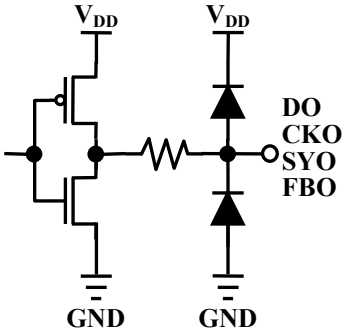
Equivalent Circuits of Input (2)



Equivalent Circuits of Inputs (3)



Equivalent Circuits of Output



Ordering Information

Part	Marking	Package	Unit per reel(pcs)
SCT2518CTSG	SCT2518CTSG	Green TSSOP24 with thermal pad	2500

StarChips Technology, Inc.

4F, No.5, Technology Rd., Science-Based Industrial Park, Hsin-Chu, Taiwan, R.O.C.

Tel : +886-3-577-5767 Ext.555,

Fax: +886-3-577-6575,

E-mail: service@starchips.com.tw

Maximum Ratings (T_A = 25°C)

Characteristic		Symbol	Rating	Unit
Supply voltage		V_{DD}	7.0	V
Input voltage		V_{IN}	-0.2 ~ V_{DD}+0.2	V
Output current		I_{OUT}	150	mA/Channel
Output voltage	Outputs	V_{OUT}	-0.2 ~ V_{DD}+0.2	V
	OUT0~OUT7		-0.2 ~ 24	V
Total GND terminals current		I_{GND}	1000	mA
Power dissipation	TSSOP24	P_D	1.56	W
Thermal resistance	TSSOP24	$R_{TH(j-a)}$	80	°C /W
Operating junction temperature		$T_{J(max)}$	150	°C
Operating temperature		T_{OPR}	-40~+85	°C
Storage temperature		T_{STG}	-55~+150	°C

The absolute maximum ratings are a set of ratings not to be exceeded. Stresses beyond those listed under "Maximum Ratings" may cause the device breakdown, deterioration even permanent damage. Exposure to the maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_A= -40 to 85°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-	3	-	5.5	V
Output voltage	V_{OUT}	Output OFF	-	-	24	V
		Output ON	1[1]	-	4[2]	V
Output current	I_{OUT}	V_{DD}=3.3/5V, V_{OUT}=0.8V	20	-	90/120	mA
		V_{DD}=3.3/5V, V_{OUT}=1V			90/140	mA
Input voltage	V_{IH}	FBI input signal	0.7V_{DD}	-	V_{DD}	V
	V_{IL}		0	-	0.3V_{DD}	V
	V_{IH}	DI/CKI/SYI/OEI/GCKI input signals	2.3	-	V_{DD}	V
	V_{IL}		0	-	0.7	V
GCKI pulse width	$t_{W(GCKI)}$	V_{DD}=3.3V/5V	2	-	-	us
OEI pulse width	$t_{W(OEI)}$	V_{DD}=3.3V/5V(GCKI NC)	20	-	-	us
		V_{DD}=3.3V/5V(with GCKI)	$t_{W(GCKI)}$	-	-	us

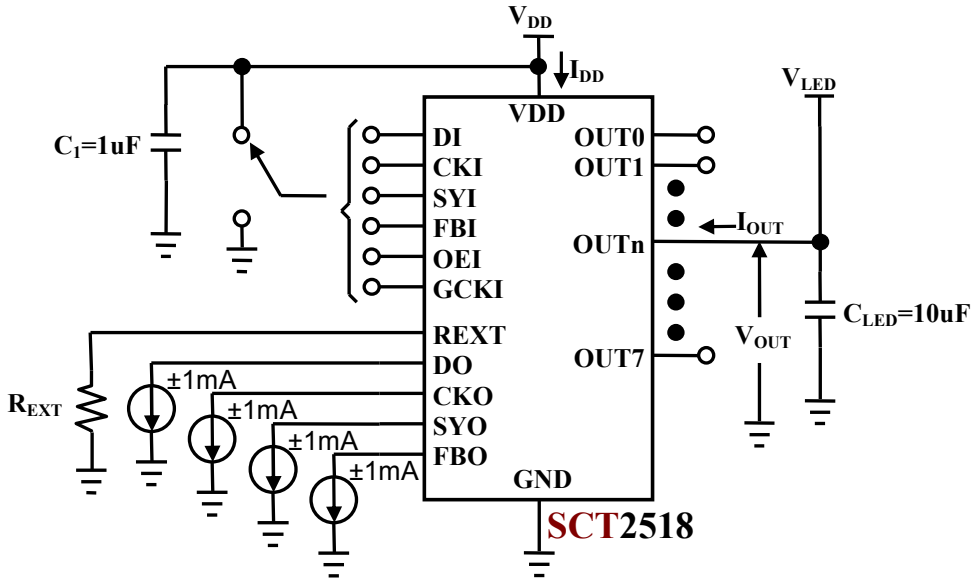
1. If V_{LED} supply voltage is under well regulation, the minimum V_{OUT} on certain output is regulated around 1V.
2. The maximum Vout is package thermal limited, user should keep Vout under maximum power dissipation.

Electrical Characteristics (V_{DD}=3.3/5V, T_A=25°C unless otherwise noted)

Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Digital inputs voltage (DI/CKI/SYI/OEI/GCKI)		V_{IH}	-	2.3	-	V_{DD}	V
		V_{IL}	-	0	-	0.7	V
FBI input voltage		V_{IH}	-	$0.7V_{DD}$	-	V_{DD}	V
		V_{IL}	-	0	-	$0.3V_{DD}$	V
Digital output voltage (DO/CKO/SYO/FBO)		V_{OH}	V_{DD}=3.3/5V, I_{OH}= -1mA	V_{DD}-0.4	-	-	V
		V_{OL}	V_{DD}=3.3/5V, I_{OL}= +1mA	-	-	0.4	V
Output leakage current		I_{OL}	V_{OUT}=24V	-	-	1	uA
Output current		I_{OUT}	V_{OUT}=1V, R_{EXT}=900Ω	-	50	-	mA
Current bit skew[1]		dI_{OUT1}	V_{OUT}=1V, R_{EXT}=900Ω	-	±1	±3	%
Chip skew[2]		dI_{OUT2}	V_{OUT}=1V, R_{EXT}=900Ω	-	±2	±6	%
Line regulation[3] I_{OUT} vs. V_{DD}		$\%/dV_{DD}$	3V<V_{DD}<5.5V, V_{OUT}>1V, R_{EXT}=900Ω	-	±0.5	±1	%/V
Load regulation[4] I_{OUT} vs. V_{OUT}		$\%/dV_{OUT}$	1V<V_{OUT}<4V, I_{OUT}=50mA, R_{EXT}=900Ω	-	±0.1	±0.5	%/V
Temp. regulation[5] I_{OUT} vs. T_A		$\%/dT_A$	-20°C < T_A < 80°C, I_{OUT}=20mA~120mA,V_{DD}=5V	-	±0.005	-	%/°C
Pull-up resistor		R_{UP}	FBI	-	200	-	KΩ
			OEI	-	180	-	KΩ
Pull-down resistor		R_{DOWN}	GCKI	-	300	-	KΩ
Thermal shutdown		T_H	Junction temperature	-	180	-	°C
		T_L		-	120	-	°C
Supply current	OFF	$I_{DD(OFF)1}$	V_{DD}=3.3/5V, R_{EXT}=Open, OUT[0:7]=OFF	-	3/4	6	mA
	OFF	$I_{DD(OFF)2}$	V_{DD}=3.3/5V, R_{EXT}=900Ω, OUT[0:7]=OFF	-	6/7	9	
	ON	$I_{DD(ON)}$	V_{DD}=3.3/5V, R_{EXT}=900 Ω, OUT[0:7]=ON	-	8/10	12	

1. Bit skew=(I_{OUT}-I_{AVG}) / I_{AVG}, where I_{AVG}=($I_{OUT(max)}$+ $I_{OUT(min)}$)/2
2. Chip skew=(I_{AVG}-I_{CEN}) / I_{CEN}*100(%), where I_{CEN} is the statistics distribution center of output currents.
3. Line regulation=[I_{OUT}(V_{DD}=5.5V)-I_{OUT}(V_{DD}=3V)] / {[I_{OUT}(V_{DD}=5.5V)+I_{OUT}(V_{DD}=3V)]/2} / (5.5V-3V)*100(%/V)
4. Load regulation=[I_{OUT}(V_{OUT}=4V)-I_{OUT}(V_{OUT}=1V)] / {[I_{OUT}(V_{OUT}=4V)+I_{OUT}(V_{OUT}=1V)]/2} / (4V-1V)*100(%/V)
5. Temperature regulation=[I_{OUT}(T_A=80°C)-I_{OUT}(T_A=-20°C)] / {[I_{OUT}(T_A=80°C)+I_{OUT}(T_A=-20°C)]/2} / (80°C+20°C)*100(%/°C)

Test Circuit for Electrical Characteristics



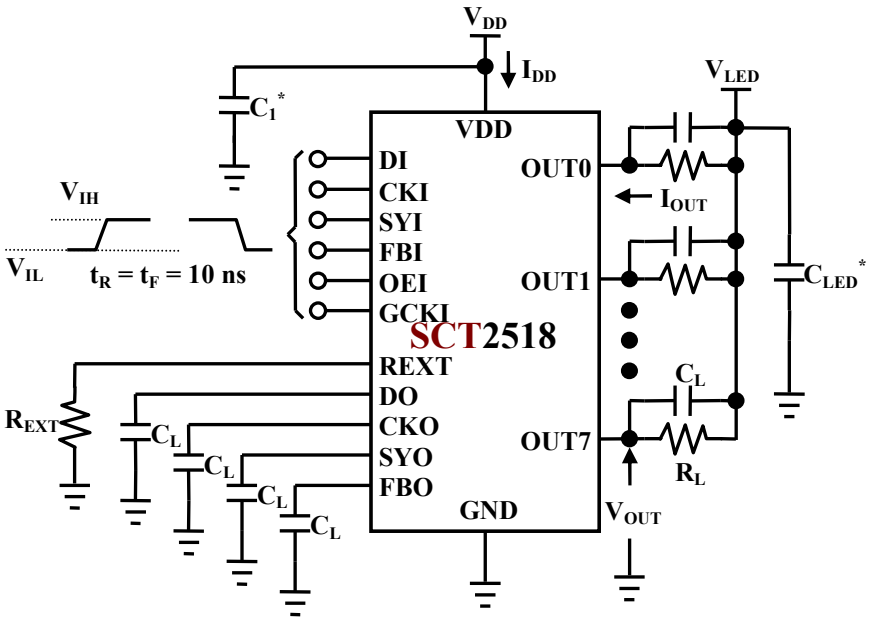
**Place C_1/C_{LED} as close to IC VDD/OUT pin(not supply source) as possible.*

Switching Characteristics (T_A=25°C unless otherwise noted)

Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time (“L” to “H”)	CKI - SYO	t_{PLH}	V_{DD} = 3.3/5V V_{LED} = 5V V_{IH} = V_{DD} V_{IL}= GND R_{EXT} = 900Ω R_L = 80Ω C_L = 10pF C_1 = 10uF C_{LED} = 100uF	-	25/20	30/25	ns
	CKI - CKO	t_{PLH1}		-	15/10	20	ns
	DI – DO	t_{PLH2}		-	15/10	20	ns
	FBI - FBO	t_{PLH3}		-	40	60	ns
Propagation delay time (“H” to “L”)	CKI - CKO	t_{PHL1}		-	15/10	20	ns
	DI - DO	t_{PHL2}		-	15/10	20	ns
	FBI - FBO	t_{PHL3}		-	40	60	ns
Pulse width	CKI	$t_{W(CKI)}$		30/25	-	-	ns
	DI	$t_{W(DI)}$		15	-	-	ns
	SYI	$t_{W(SYI)}$		15	-	-	ns
	GCKI	$t_{W(GCKI)}$		2	-	-	us
	OEI	$t_{W(OEI)}$		20	-	-	us
				$t_{W(GCKI)}$[2]	-	-	us
	SYO	$t_{W(SYO)}$		100	-	-	ns
Setup time for DI		$t_{S(DI)}$		5	-	-	ns
Hold time for DI		$t_{H(DI)}$		10	-	-	ns
Setup time for SYI		$t_{S(SYI)}$		20	-	-	ns
Output rise time (DO/CKO/SYO/FBO)		t_{OR}		-	20	-	ns
Output fall time (DO/CKO/SYO/FBO)		t_{OF}		-	20	-	ns
Maximum CKI rise time[1]		t_R		-	-	5	us
Maximum CKI fall time		t_F		-	-	5	us
PWM Clock Frequency		f_{OSC}	-	-	120/100	-	KHz

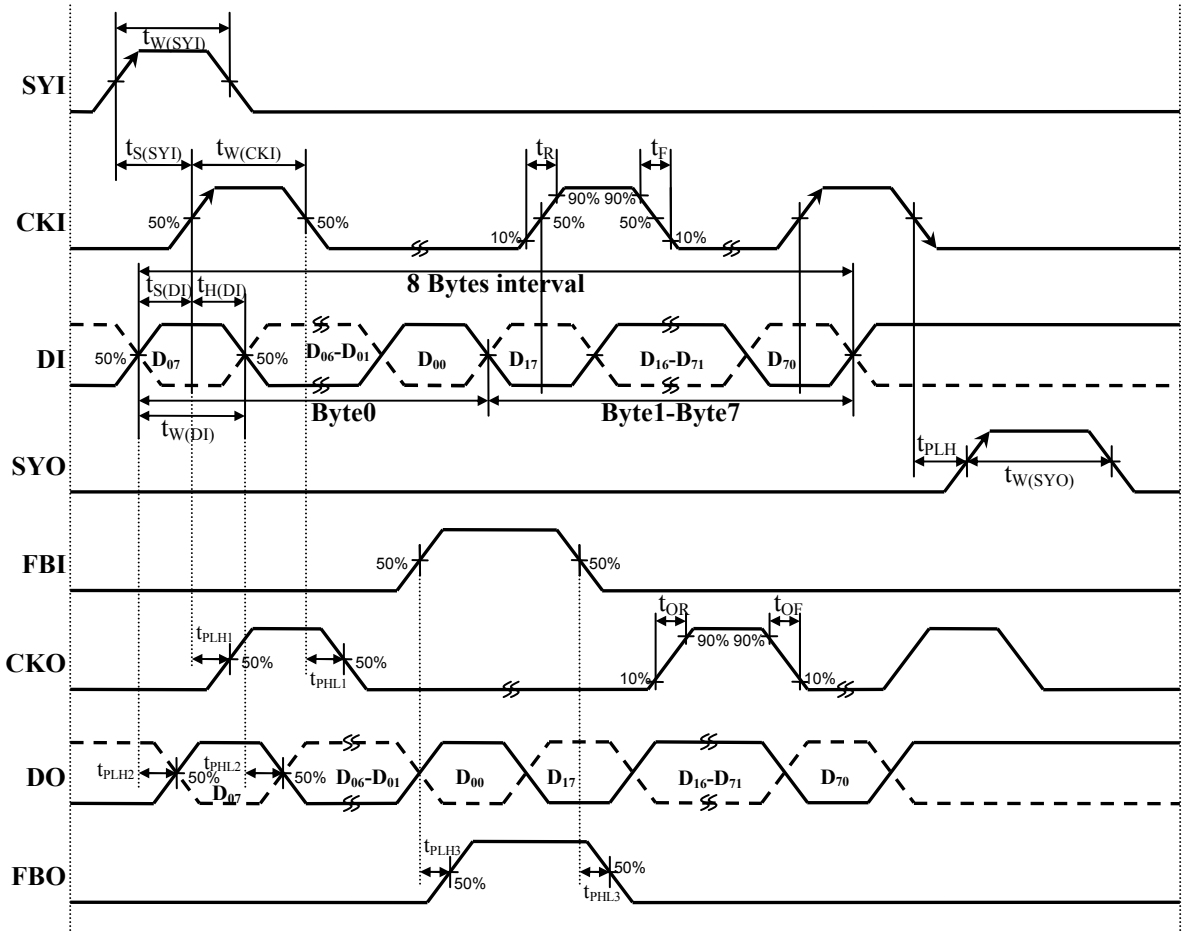
1. It may not be possible to achieve the timing required for data transfer between two cascaded drivers if t_R/t_F is large.
2. This item takes effect if external PWMCLK is applied.

Test Circuit for Switching Characteristics



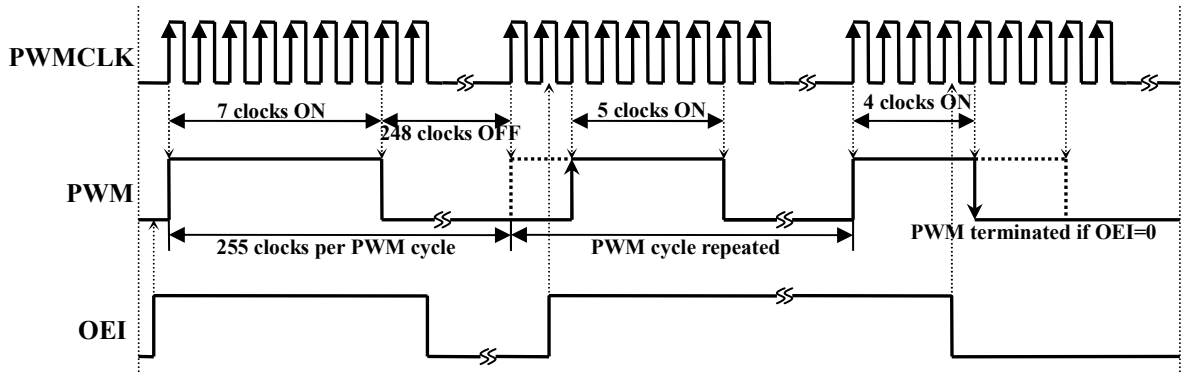
Place C_1/C_{LED} as close to IC VDD/OUT pin(not supply source) as possible.

Timing Waveform

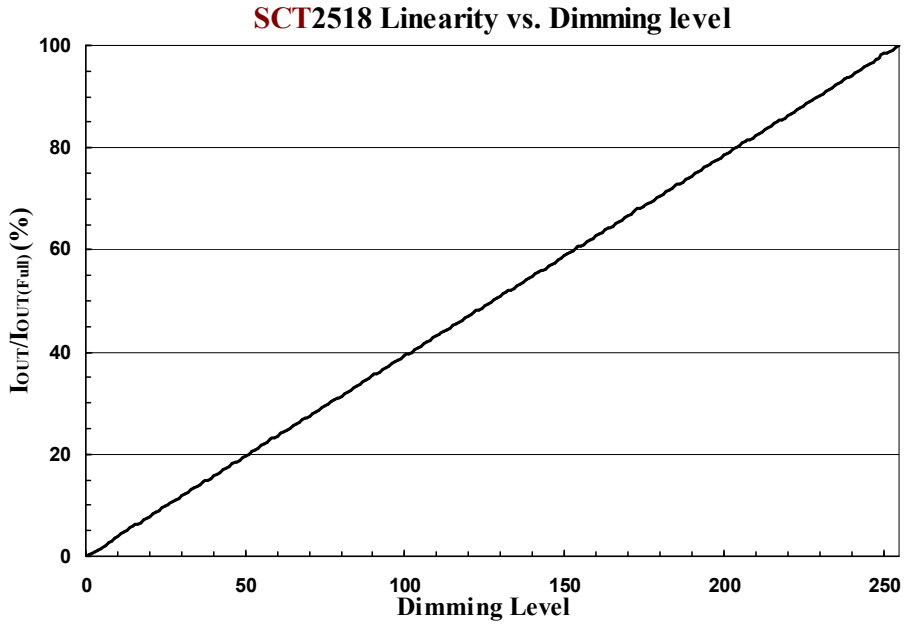


8-bit PWM

PWM luminance data code D = (D7, D6, D5, D4, D3, D2, D1, D0) determines duty of the output turn-on pulse = $(D7*2^7+D6*2^6+D5*2^5+D4*2^4+D3*2^3+D2*2^2+D1*2^1+D0*2^0)/255$. For example when D = $00000111_B = 7_D$, the output will be turned on for a time interval by counting 8-bit counter from binary code 0000_B to 0110_B (D-1) through internal PWM clock PWMCLK. That is, when OEI is active, the output will turn on for 7 PWM clocks of total 255 clock cycles over and over. Such a turn-on status will last until the 8-bit latch is loaded with new luminance data code. When D = 0/255 the output will be fully turned off/on without PWM functionality. The output of SCT2518 is initialized to be ON. This makes the LED backlight source automatically lit-up even if controller doesn't issue any signals to the SCT2518.



The figure shown below is the dimming characteristics of on-system testing. The result exhibits excellent output current linearity with PWM dimming level from 0 to 255(full gray scale). Even at low gray PWM level the LED string does not flicker.

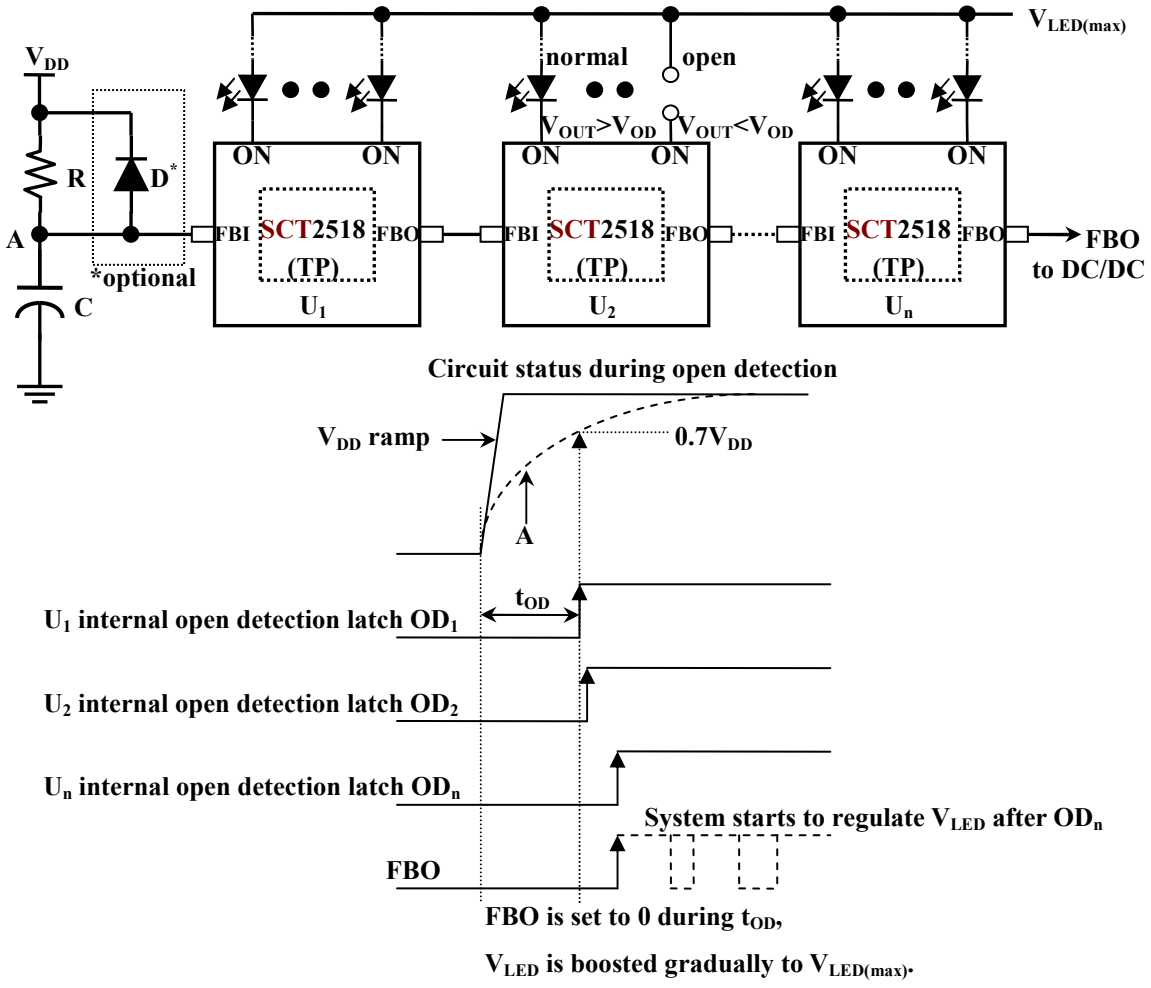


Power-on Open Detection

To prevent system feedback from abnormal operation when LED strings are not connected to driver, the SCT2518 performs one-time open detection when driver is powered on. User should set sufficient open detection time t_{OD} by applying proper RC delay setting at FBI pin of first IC U_1. The scheme of power-on open detection is described as below:

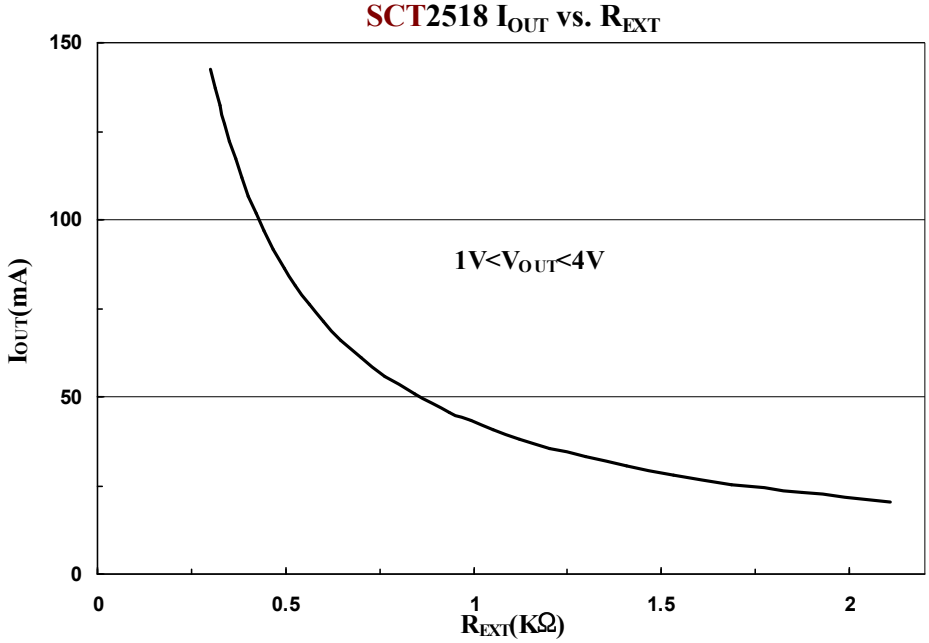
When system is powering on, outputs of each driver are mandatory tuned on and FBO is forced to 0 for a period of time. The time determined by point A is reached to around $0.7V_{DD}$. The V_{LED} should be boosted gradually to $V_{LED(max)}$ if DC/DC is well operated and RC time constant is sufficient. Once the LED string is open, the V_{OUT} is generally less than V_{OD}(~0.3V) with output ON condition. At $t=t_{OD}$, the internal OD_1 rising edge of first IC will latch the status of IC_1's output port. After IC_1 OD (open detection) code is latched, the FBO is transmitted to next IC, then IC_2 starts to detect its OD code according to IC_2's output status. The same detection is applied to subsequent ICs, until all ICs are performed open detection. The open ports will not be taken into consideration on LED supply regulation.

The t_{OD} time must be greater than the time for V_{LED} to reach to $V_{LED(max)}$, yet not too long to induce thermal shutdown happened. As a rule of thumb, RC time constant of around 0.1s with, e.g., R=22K, C=4.7u is usually sufficient for generic DC/DC converter system. Please adapt RC according to your system. Furthermore, an optional fast discharge path by adding a diode to V_{DD} could also be considered.



Adjusting Output Current

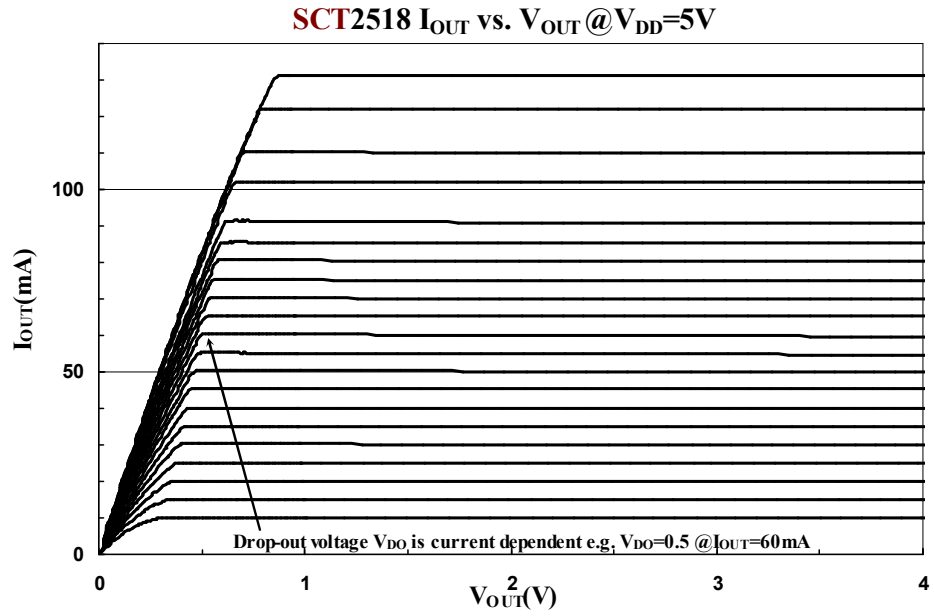
The SCT2518's output current (I_{OUT}) are set by one external resistor at pin REXT. The output current I_{OUT} versus resistance of R_{EXT} is shown as the following figure.

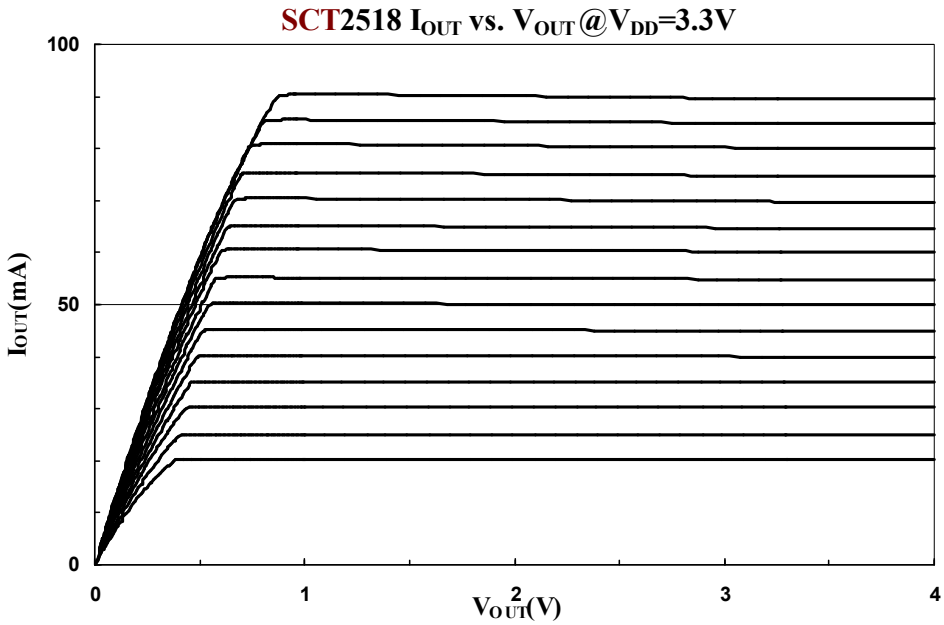


Furthermore, when SCT2518's output voltage is set between 1 Volt and 4 Volt, the output current can be estimated approximately by: $I_{OUT} = 68(660 / R_{EXT})$ (mA) (chip skew < ±6%). Thus the output current is set to be about 50mA at R_{EXT} = 900Ω.

Output Characteristics

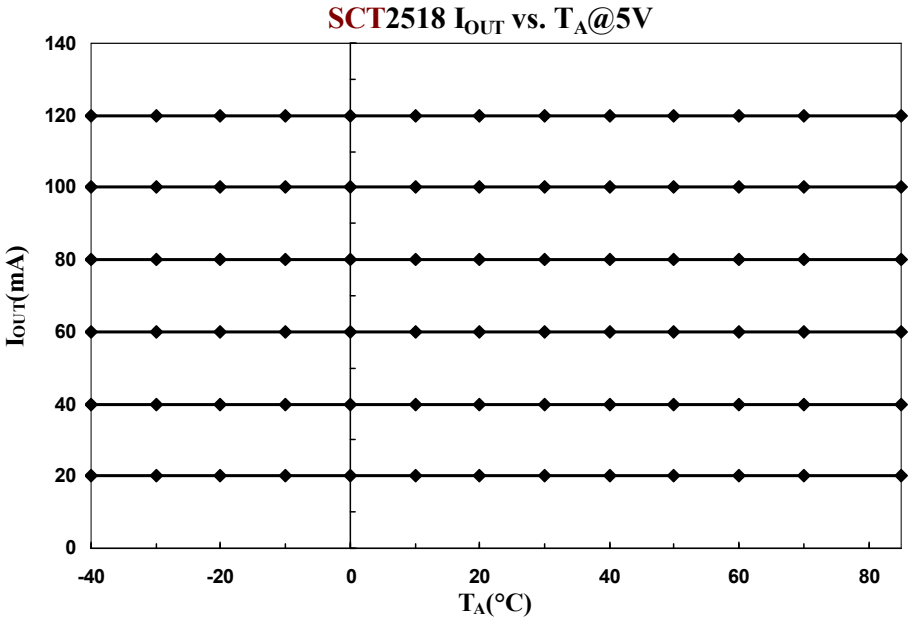
The current characteristic of output curve is flat. The output current can be kept constant regardless of the variations of LED forward voltage when $V_{OUT} > V_{DO}$. The relationship between I_{OUT} and V_{OUT} is shown below. The output voltage should be kept as low as possible to prevent the SCT2518 from being overheated.





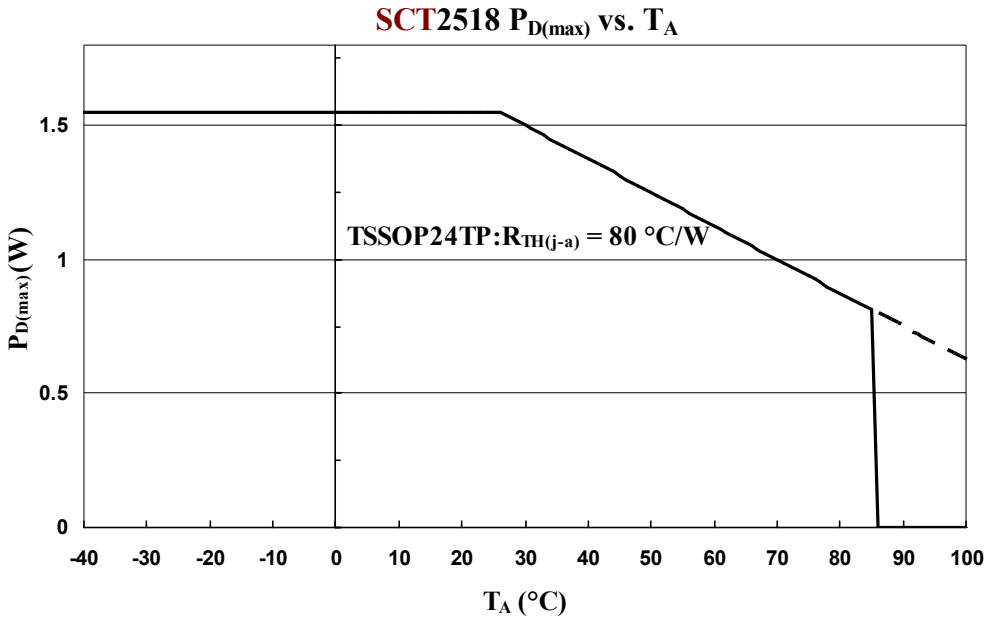
Excellent Temperature Regulation

The constant current driver requires not only the characteristics of supply and load voltage independence, but also temperature invariance. A well thermal stable reference circuit is designed within the SCT2518. Users can get the stable output current over recommended current range I_{OUT}=20mA~120mA with ambient temperature (T_A) widely varying from -40°C to 85°C.



Power Dissipation

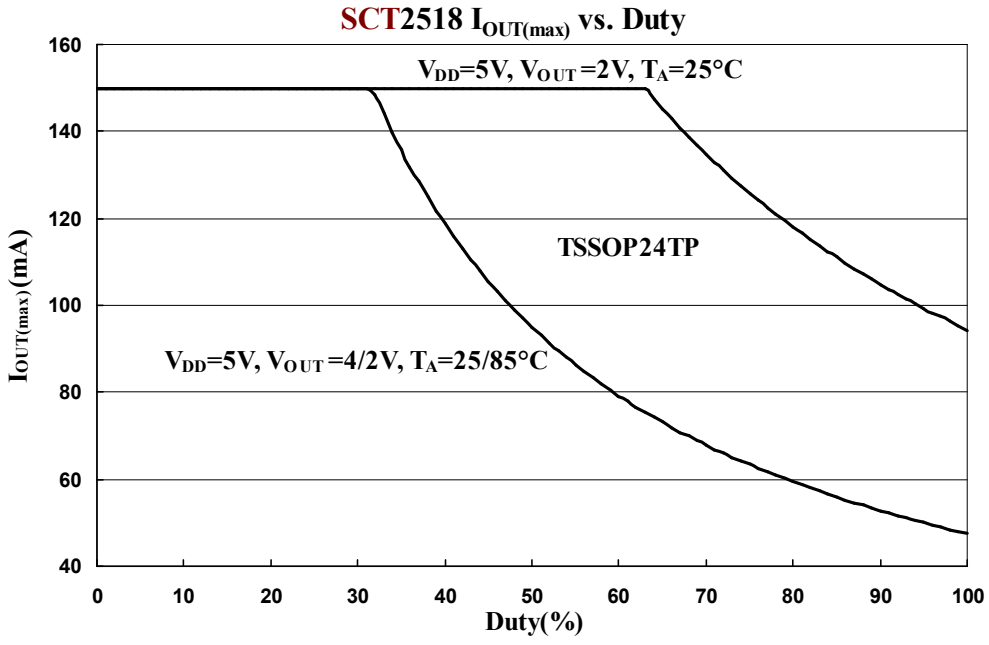
The maximum power dissipation ($P_{D(max)}$) of a semiconductor chip varies with different packages and ambient temperature. It's determined as $P_{D(max)}=(T_{J(max)} - T_A)/R_{TH(j-a)}$ where $T_{J(max)}$: maximum chip junction temperature is usually considered as 150°C, T_A: ambient temperature, $R_{TH(j-a)}$: thermal resistance. Since P=IV, for sinking larger I_{OUT}, users had better add proper voltage reducers on outputs to reduce the heat generated from the SCT2518.



Limitation on Maximum Output Current

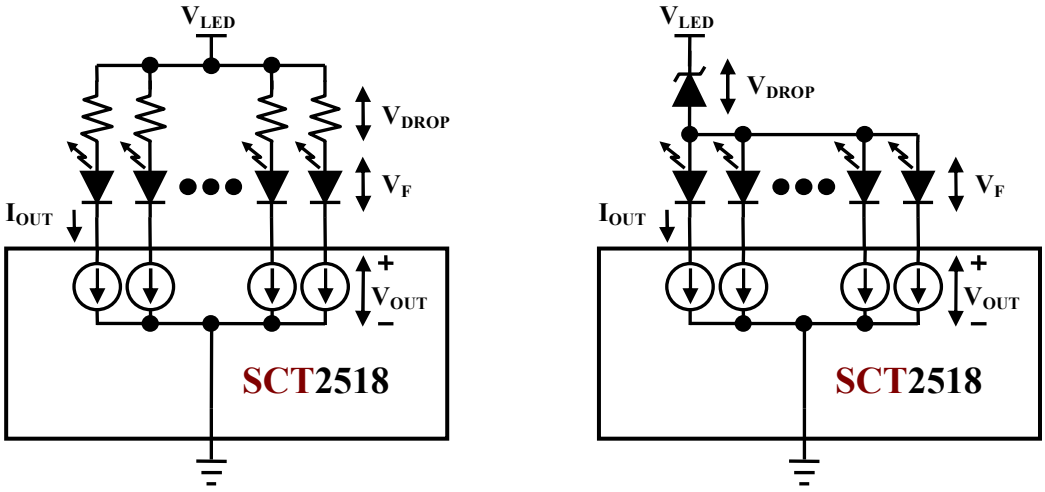
The maximum output current vs. duty cycle is estimated by:

$I_{OUT(max)}=(((T_{J(max)}-T_A)/R_{TH(j-a)})-(V_{DD}*I_{DD}))/V_{OUT}/Duty/N$ where $T_{J(max)}$=150°C, N=8(all ON)



Load Supply Voltage (VLED)

The SCT2518 can be operated very well when V_{OUT} ranges from 1V to 4V. However, it is recommended to use the lowest possible supply voltage or set a voltage reducer to reduce the V_{OUT} voltage, at the same time reduce the power dissipation of the SCT2518. This can prevent the IC from malfunction with thermal shutdown situation. Follow the diagram instructions shown below to lower down the output voltage. This can be done by adding additional resistor or zener diode, thus $V_{OUT}=V_{LED}-V_{DROP}-V_F$.



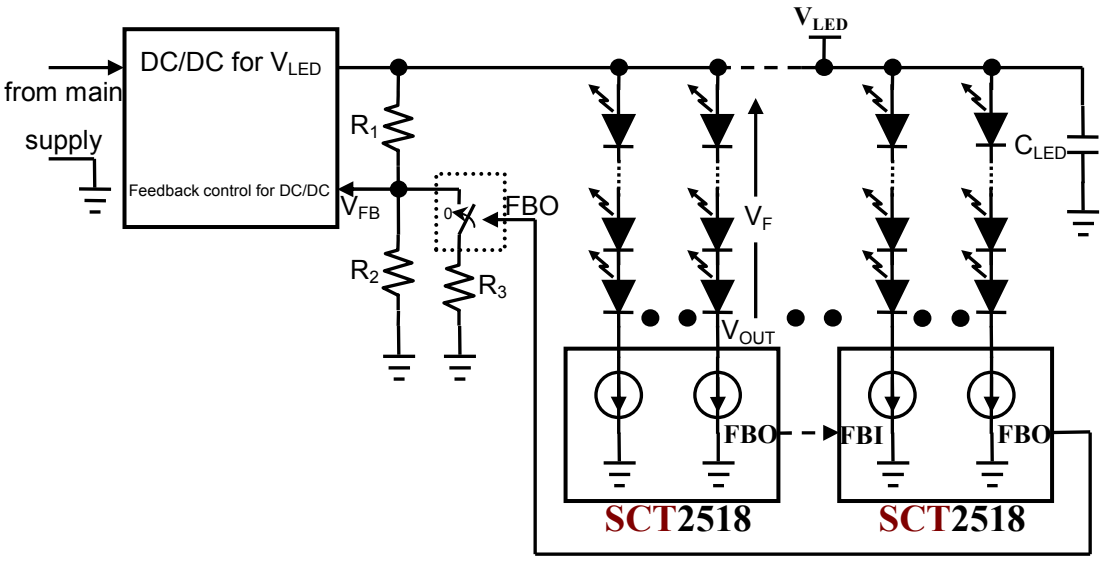
Over Temperature Shutdown

The SCT2518 contains thermal shutdown scheme to prevent damage from being over heated. The internal thermal sensor turns off all outputs when the die temperature exceeds +180°C. The outputs are enabled again when the die temperature drops below +120°C. During the thermal shutdown process, the LEDs look blinking since it is turned OFF then ON periodically.

Typical Application

V_{LED} Supply Regulation Feedback

In order to reduce the total system power dissipation due to LED V_F skew, the SCT2518 incorporates feedback function to detect the minimum V_{OUT}, thus the minimum required supply voltage V_{LED} for the LED strings can be automatically regulated. The concept shown below can be applied to off-the-shelf DC/DC converter or LDO with adjustable output voltage.



The function of this circuit is as follows:

When any of V_{OUT} is less than internal setting voltage 1V (the voltage is applicable for most current range), the last cascaded FBO to DC/DC is set to '0'. The turn on switch will decrease the equivalent R2, the VFB is pulled down toward lower voltage. The DC/DC compensates the LED supply voltage by increasing the voltage on V_{LED}. Users should be aware of the regulation loop for stability issue. Otherwise, the LED may flick due to, e.g., larger V_{LED} ripple or noise induced DC/DC entering protection mode which takes time to re-start the control loop. When designing the resistors R_1~R_3, user should consider the V_F skew distribution as well as 1V the SCT2518 driver needs:

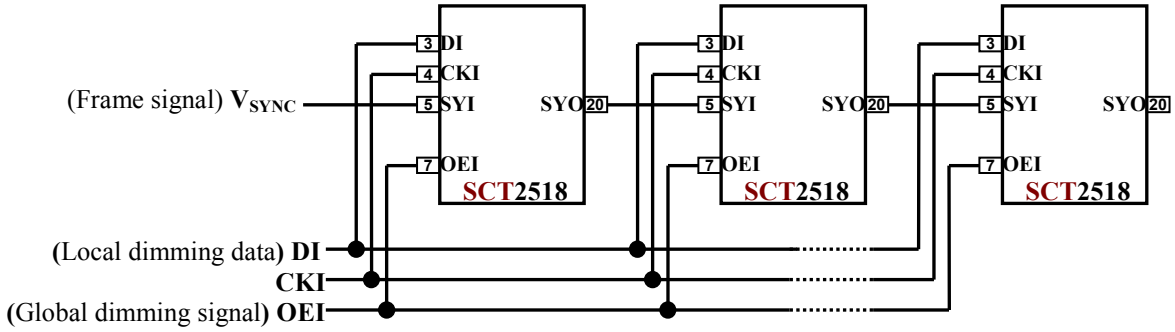
$V_{LED(min)} = V_{REF}*(1+R_1/R_2)$

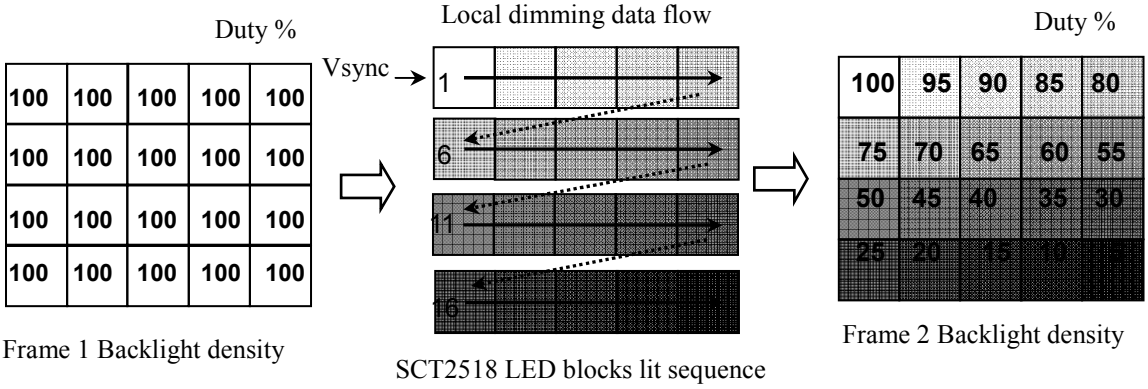
$V_{LED(max)} = V_{REF}*(1+R_1/(R_2//R_3))$, where V_{REF} is reference voltage of DC/DC converter.

Therefore, the optimum V_{LED} is automatically regulated between $V_{LED(min)}$~$V_{LED(max)}$ according to LED string. Even if the LED strings are broken or some LEDs are shorted, the supply always stays within the limits. Since the total V_F of each LED string is different and all LED strings load are tied to the same supply voltage V_{LED}, thus $V_{OUT(min)}=V_{LED}-V_{F(max)}$ and $V_{OUT(max)}=V_{LED}-V_{F(min)}$. If V_F skew is too large, an over-heated situation occurs, therefore thermal shutdown happens.

Dimming with internal PWM clock

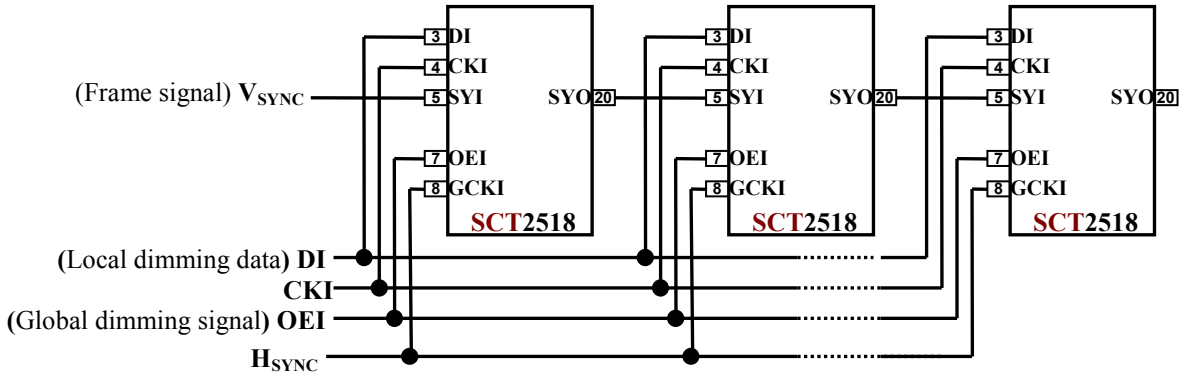
In application of LCD backlight, the SCT2518s can be daisy chained to drive LED blocks with local dimming function in sequence of scanning images. A synchronous signal V_{SYNC} initiated from controller is used to identify a frame start. The SCT2518 receiving the V_{SYNC} signal from the SYI pin has the right to download the PWM data bytes. Once the 8 PWM data are placed into the 8 data latches (8X8 bits), the V_{SYNC} signal is passed to the next SCT2518 via the SYO pin. Thus the brightness of each LED block is adjusted in proper status and LEDs are lit according to the luminance of each block's image.



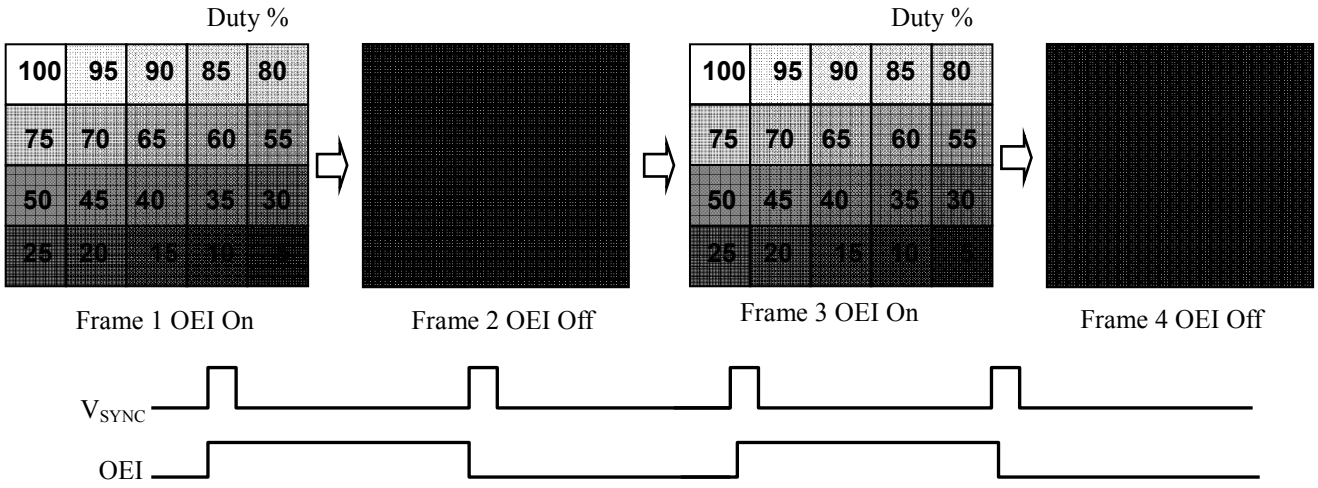


Dimming with external PWM clock (Hsync signal)

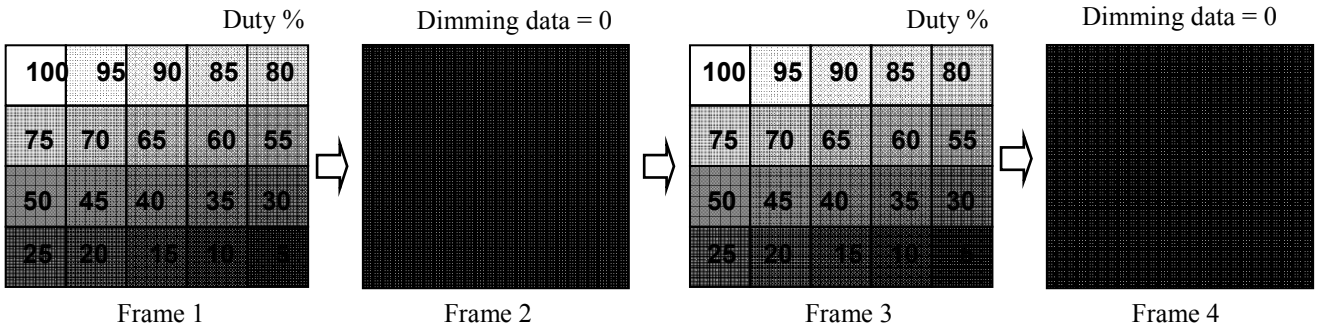
Each SCT2518 has its own oscillator, in case of GCKI is grounded. The built-in internal 100K Hz PWM clock signal is employed for PWM function. The PWM clock is automatically switched to external clock once the pin GCKI detects the rising edge, and thus the synchronization of PWM clock signal is achieved between the SCT2518s.



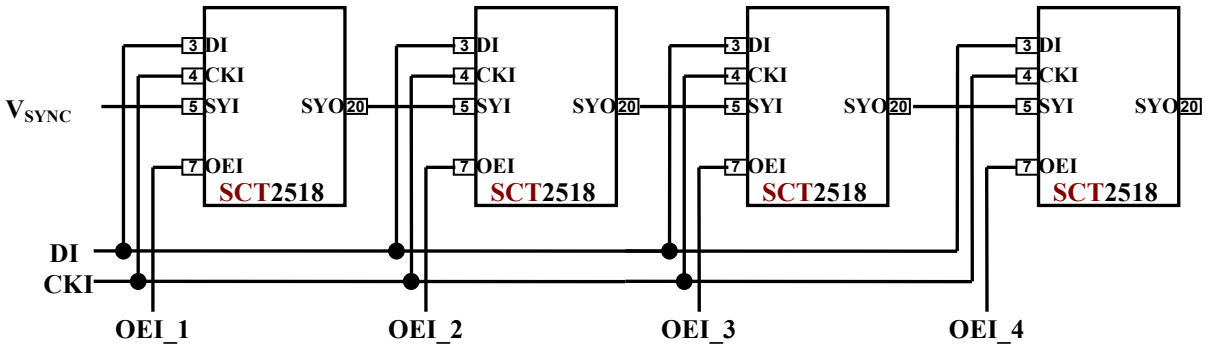
Dimming with black frame insertion (by EOI signal)

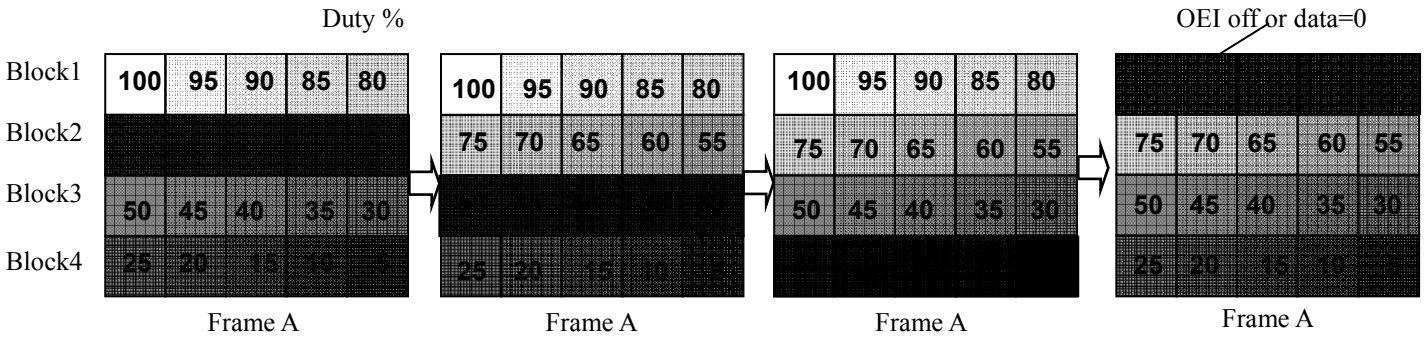


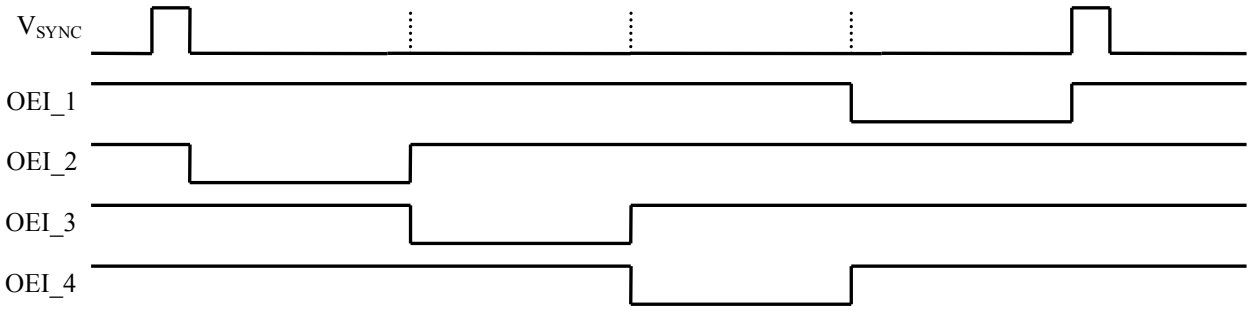
Dimming with black frame insertion (by dimming data)



Dimming with blocks scanning (by OEI or data signals)





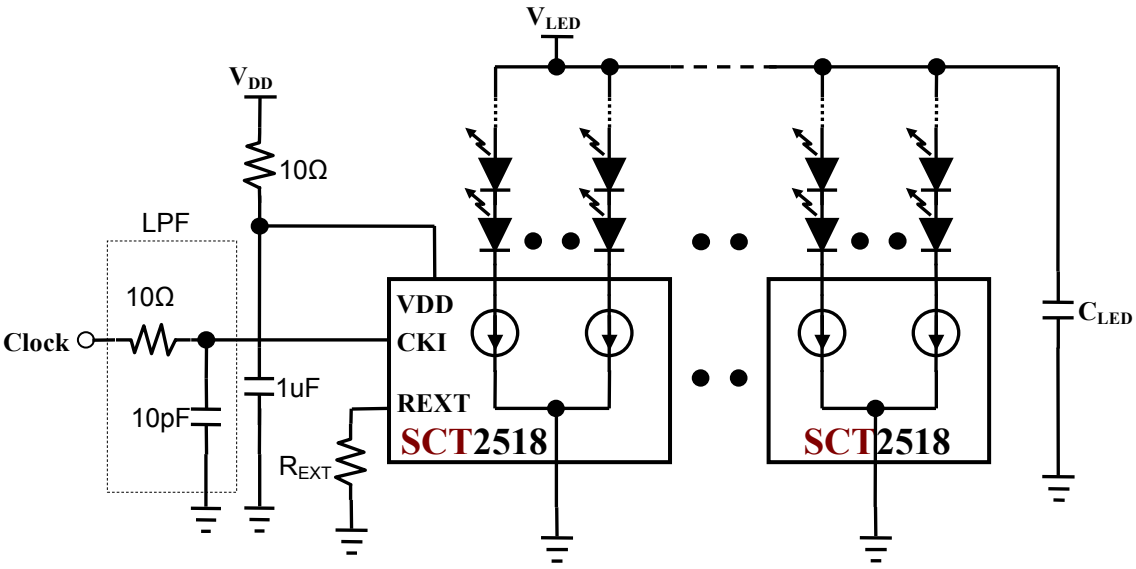


PCB Design Considerations

Use the following general guide-line when designing printed circuit boards (PCB):

Decoupling Capacitor

Place a decoupling capacitor, e.g., 1uF between VDD and GND pins of SCT2518. Locate the capacitor as close to the SCT2518 as possible. The necessary capacitance depends on the LED load current, PWM switching frequency, and serial-in data speed. Inadequate VDD decoupling can cause timing problems, and very noisy LED supplies can affect LED current regulation.



External Resistor (R_{EXT})

Locate the external resistor as close to the REXT pin as possible to avoid the noise influence.

Power and Ground

Maximizing the width and minimizing the length of VDD and GND trace improves efficiency and ground bouncing by effect of reducing both power and ground parasitic resistance and inductance. A small value of resistor, e.g., 10Ω (higher if I_{OUT} is larger) series in power input of the SCT2518 in conjunction with decoupling capacitor shunting the IC is recommended. Separating and feeding the LED power from another stable supply terminal V_{LED}, furthermore adding a capacitor C_{LED} greater than 10uF beside the LED are recommended. Please adapt C_{LED} according to total system current consumption.

EMI Reduction

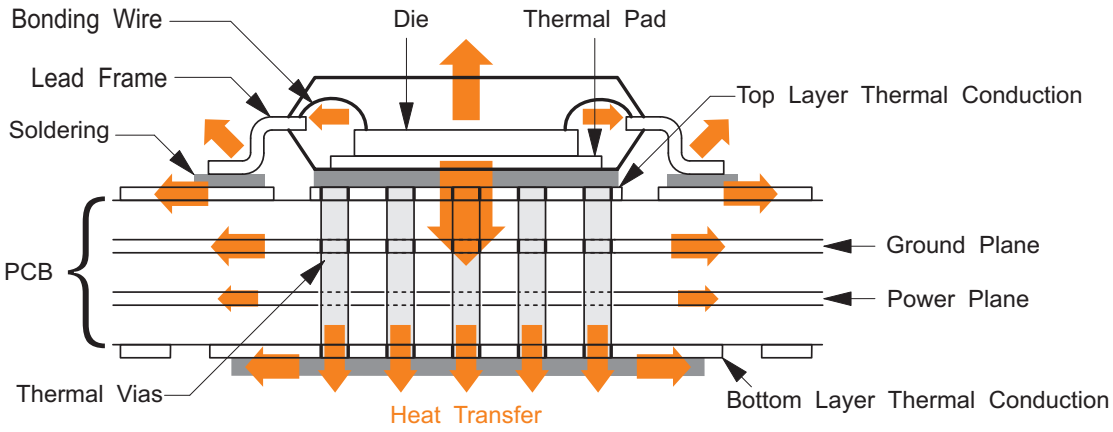
To reduce the EMI radiation from system, an economical solution of RC low pass filter (LPF) is suggested to be used to lower the transient edge of clock input signal, as shown in the figure above. Using at least four layers PCB board with two interior power and ground planes is a good scheme to decrease the signal current path which is the source of radiation emission. As a result, EMI radiation can be decreased.

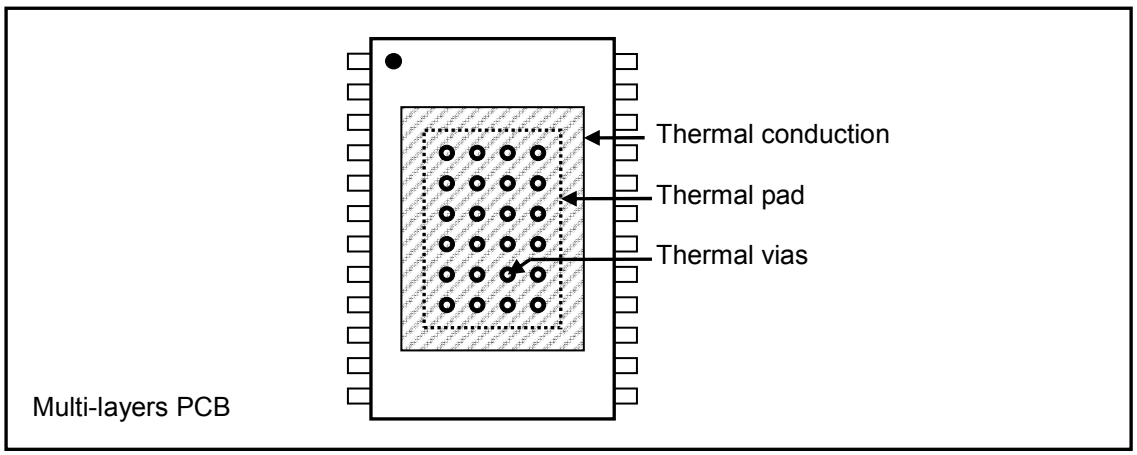
Thermal Pad Consideration

The “thermal pad” (also named as “exposed pad”) TSSOPTP package beneath used to increase the heat dissipation capability is grounded. User should be aware of this electrical connection when designing the PCB board, and make provisions for its use. In most of application, the thermal pad is electrically connected to ground plane or conduction. This makes the IC operated with more stable condition.

In general, the heat generated from an IC is conducted to the PCB then radiates to the ambient. Thermal pad specifically increases the maximum power dissipation capability of the IC packages. To provide lower thermal resistance from the IC to the ambient air, PCB designers should layout larger thermal conduction areas on top layer (component side) and bottom layer (solder side) as well as thermal vias, the more the better. In addition, connecting thermal via to the ground plane also increases thermal conduction areas, this improves the heat transfer efficiency at the same time greatly dissipates heat generated from the package. Furthermore, coating solder on bottom layer and selecting, e.g., 2 oz. copper which will increase the total thickness of thermal conduction is an alternative.

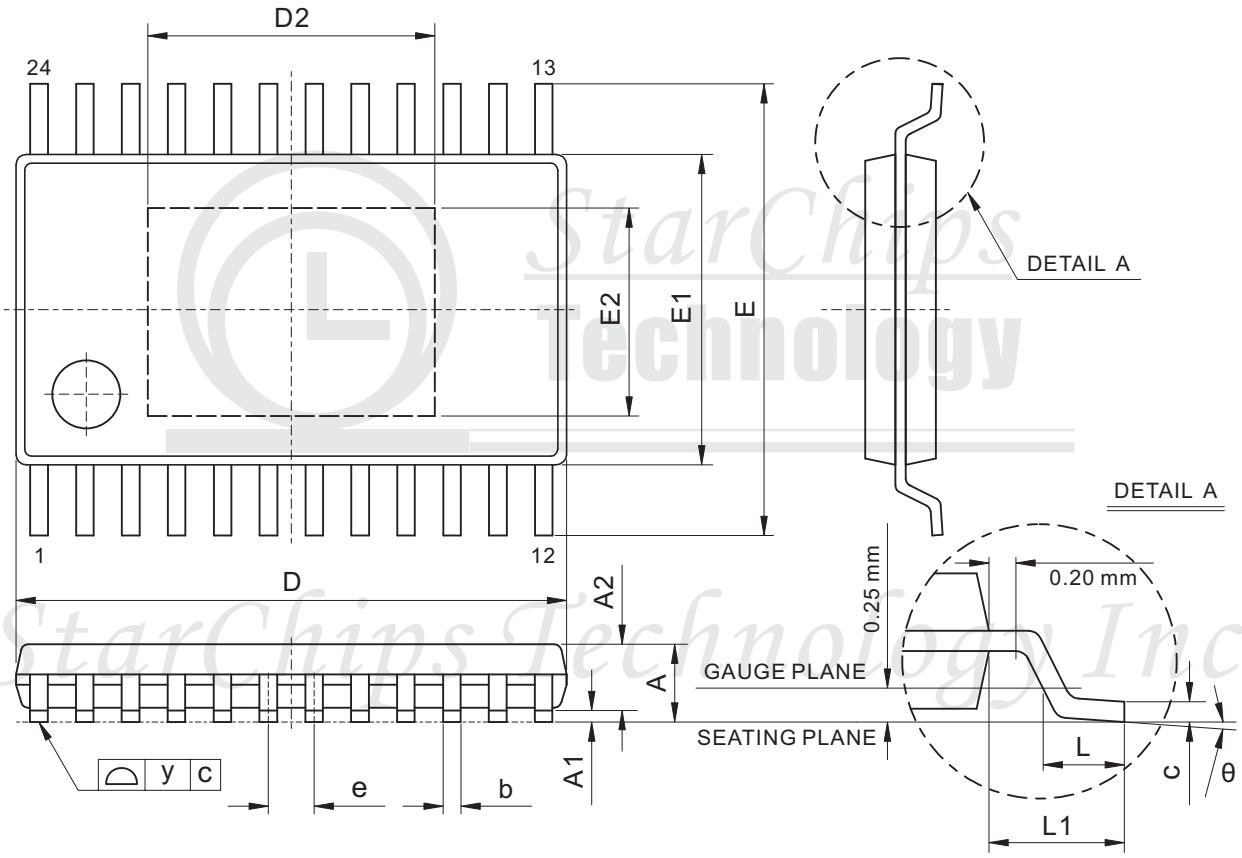
When making the solder paste screen, an opening should be created for the thermal pad. This way the thermal pad can be electrically and thermally connected to the PCB. As the thermal pad is soldered on copper polygon, the chance of inadvertently shorting the thermal pad to traces routed underneath it could be eliminated.





Package Dimension

TSSOP24TP(check up-to-date version)



Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.20	-	-	47.0
A1	0.05	-	0.15	2.0	-	6.0
A2	0.80	0.90	1.05	31.0	35.0	41.0
b	0.19	-	0.30	7.0	-	12.0
c	0.09	-	0.20	4.0	-	8.0
D	7.70	7.80	7.90	303.1	307.1	311.0
E1	4.30	4.40	4.50	169.0	173.0	177.0
E	6.40 BSC			252.0 BSC		
e	0.65 BSC			26.0 BSC		
L1	1.00 REF			39.0 REF		
L	0.45	0.60	0.75	18.0	24.0	30.0
y	-	-	0.10	-	-	4.0
θ	0°	-	8°	0°	-	8°
D2	-	4.57	-	-	180.0	-
E2	-	3.00	-	-	118.0	-

Revision History (check up-to-date version)

Data Sheet Version	Remark
V01_03	Skew spec. updated; open detection added

Information provided by StarChips Technology is believed to be accurate and reliable. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Starchips can not assume responsibility and any problem raising out of the use of the circuits. Starchips reserves the right to change product specification without prior notice.