8-Channel Constant Current Driver

Product Description

The SCT2008S is an eight channels constant current driver best for LED lighting. It provides the PWM control effect by sinking constant current from LED clusters with minimum pulse width 200ns. The PWM control is performed by connecting the PWM signal from system control unit to OE pin of the SCT2008S. The full scale current value of each output is set by an external resistor connected to REXT pin.
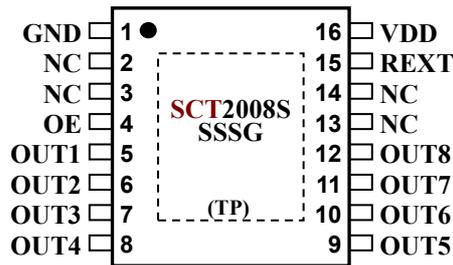
The SCT2008S guarantees to endure maximum DC 24V at each output port. Each output of SCT2008S can sink a constant current up to 90mA. Users can simply shunt the outputs to get higher current driver-ability, especially in the case of high power LED lighting.

The excellent current regulation capability allows SCT2008S easily drive each output current to a constant stable output nearly without affected by power supply of LED, loading due to variant V_F of LEDs and operating temperature. The SCT2008S is equipped with over temperature protection. The eight channels IC stops driving the output while junction temperature exceeds 160°C the high limit and the output will be reactivated while the junction temperature is below 110°C the low limit. In conclusion, the driver system is protected from damage of overheated.

Features

- ◆ Eight constant-current outputs rate at 24V
- ◆ Constant current range: 10 – 60/90mA@3.3/5V
- ◆ Excellent regulation to load, supply voltage and temperature
- ◆ Minimum PWM pulse width 200ns
- ◆ ±2%(typ) current matching between outputs
- ◆ ±4%(typ) current matching between ICs
- ◆ Dropout output 0.5V@40mA,V_{DD}=5V
- ◆ Two steps current ramp to lower output switching noise
- ◆ All output current are adjusted through one external resistor
- ◆ Built-in power on reset and thermal protection
- ◆ Supply voltage range 3.3 to 5V
- ◆ Dimming control with Schmitt triggered input
- ◆ Package: SSOP16 with heat sink pad
- ◆ Application: LED backlight, LED lighting, LED lamp

Pin Configuration

```
        GND  ┌1 ●        16┐ VDD
        NC   ┌2          15┐ REXT
        NC   ┌3  SCT2008S 14┐ NC
        OE   ┌4   SSSG    13┐ NC
        OUT1 ┌5          12┐ OUT8
        OUT2 ┌6          11┐ OUT7
        OUT3 ┌7  (TP)    10┐ OUT6
        OUT4 ┌8           9┐ OUT5
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Terminal Description

Pin Name	Pin No.	I/O	Function
GND	1	-	Ground terminal
NC	2,3,13,14	-	No connection
OE	4	I	Input terminal of output enable signal. Output is enabled when OE is high.
OUT1~8	5~12	O	Output terminals with constant current
REXT	15	I/O	Input terminal connected to an external resistor for setting up all output current
VDD	16	-	Supply voltage terminal
TP	TP		Thermal pad, please connect TP to ground.

Block Diagram
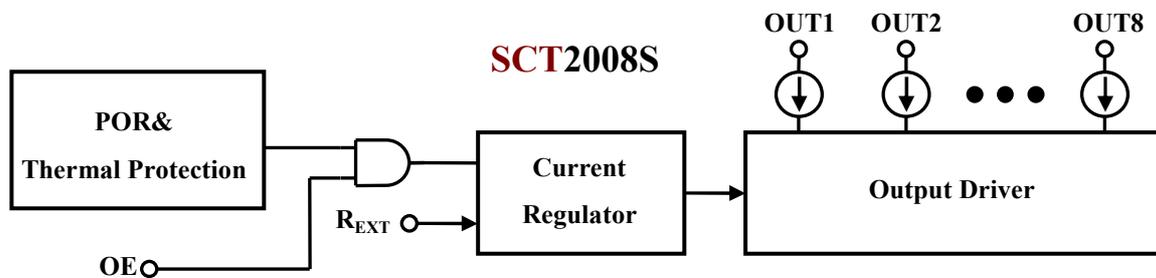
Equivalent Circuits of Inputs
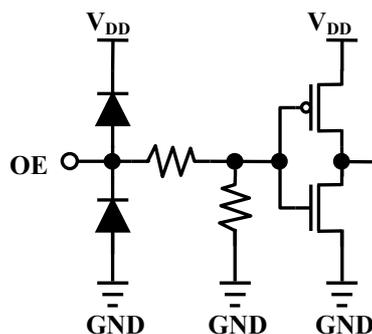
Ordering information

Part	Marking	Package	Unit per reel(pcs)
SCT2008SSSG	SCT2008SSSG	Green SSOP16(150mil) with thermal pad	2500

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Maximum Ratings $(T_A = 25°C)$

Characteristic		Symbol	Rating	Unit
Supply voltage		V_{DD}	7	V
Input voltage		V_{IN}	$-0.2 \sim V_{DD}+0.2$	V
Output current		I_{OUT}	100	mA/Channel
Output voltage		V_{OUT}	24	V
Total GND terminals current		I_{GND}	800	mA
Power dissipation	SSOP16TP	P_D	2.08	W
Thermal resistance	SSOP16TP	$R_{TH(j-a)}$	60	°C /W
Operating temperature		T_{OPR}	$-40\sim+85$	°C
Storage temperature		T_{STG}	$-55\sim+150$	°C

The absolute maximum ratings are a set of ratings not to be exceeded. Stresses beyond those listed under "Maximum Ratings" may cause the device breakdown, deterioration even permanent damage. Exposure to the maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions $(T_A=-40$ to $85°C$ unless otherwise noted)

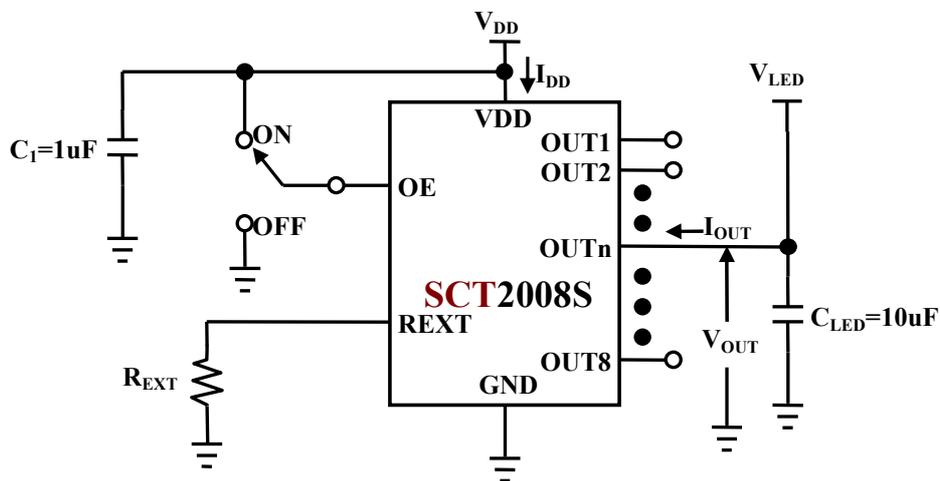| Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-	3	-	5.5	V
Output voltage	V_{OUT}	Output OFF	-	-	24	V
		Output ON	-	1	4	V
Output current	I_{OUT}	DC test circuit	10	-	60/90	mA
Input voltage	V_{IH}	-	$0.7V_{DD}$	-	V_{DD}	V
	V_{IL}	-	0	-	$0.3V_{DD}$	V
OE pulse width	t_w	V_{DD}=3.3-5V	200	-	-	ns

1. The output current keep constant in range of 10-90mA if V_{OUT}=1V.
    However, user can minimize V_{OUT} to reduce power dissipation according to used current, e.g., set V_{OUT} to 0.6V if I_{OUT}=40mA.
2. The maximum Vout is package thermal limited, user should keep Vout under maximum power dissipation.

Electrical Characteristics $(V_{DD}=3.3/5V, T_A=25°C$ unless otherwise noted)

Characteristic		Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage		V_{IH}	-		$0.7V_{DD}$	-	V_{DD}	V
		V_{IL}	-		0	-	$0.3V_{DD}$	V
Output leakage current		I_{OL}	V_{OUT} = 24V		-	-	0.5	uA
Output current		I_{OUT}	V_{OUT}=1V	R_{EXT}=900Ω	-	42	-	mA
Current channel skew[1]		dI_{OUT1}	V_{OUT}=1V	R_{EXT}=900Ω	-	±2	±3	%
Current chip skew[2]		dI_{OUT2}	V_{OUT}=1V	R_{EXT}=900Ω	-	±4	±6	%
Line regulation I_{OUT} vs. V_{DD}[3]		$\%/dV_{DD}$	$3V < V_{DD} < 5.5V$ R_{EXT}=900Ω, V_{OUT} > 1V		-	±0.5	±1	%/V
Load regulation I_{OUT} vs. V_{OUT}[4]		$\%/dV_{OUT}$	$1V < V_{OUT} < 4V$, R_{EXT}=900Ω, V_{DD}=3.3-5V		-	±0.5	±1	%/V
Pull-down resistor		R_{DOWN}	OE		-	400	-	KΩ
Thermal shutdown		T_H	Junction Temperature		-	160	-	°C
		T_L			-	110	-	°C
Supply current	OFF	$I_{DD(OFF)1}$	R_{EXT} = Open, OUT_1~OUT_8=OFF		-	3	5	mA
		$I_{DD(OFF)2}$	R_{EXT} = 900Ω, OUT_1~OUT_8=OFF		-	6	8	
	ON	$I_{DD(ON)}$	R_{EXT} = 900Ω, OUT_1~OUT_8=ON		-	8	10	

1. Bit skew=$(I_{OUT}-I_{AVG})$ / I_{AVG}, where $I_{AVG}=(I_{OUT(max)}+ I_{OUT(min)})/2$
2. Chip skew=$(I_{AVG}-I_{CEN})$ / I_{CEN}*100(%), where I_{CEN} is the statistics distribution center of output currents.
3. Line regulation=$[I_{OUT}(V_{DD}=5.5V)-I_{OUT}(V_{DD}=3V)]$ / $\{[I_{OUT}(V_{DD}=5.5V)+I_{OUT}(V_{DD}=3V)]/2\}$ / (5.5V-3V)*100(%/V)
4. Load regulation=$[I_{OUT}(V_{OUT}=4V)-I_{OUT}(V_{OUT}=1V)]$ / $\{[I_{OUT}(V_{OUT}=4V)+I_{OUT}(V_{OUT}=1V)]/2\}$ / (4V-1V)*100(%/V)

# Test Circuit for Electrical Characteristics

## Switching Characteristics $(V_{DD}=3.3/5V, T_A=25°C$ unless otherwise noted)

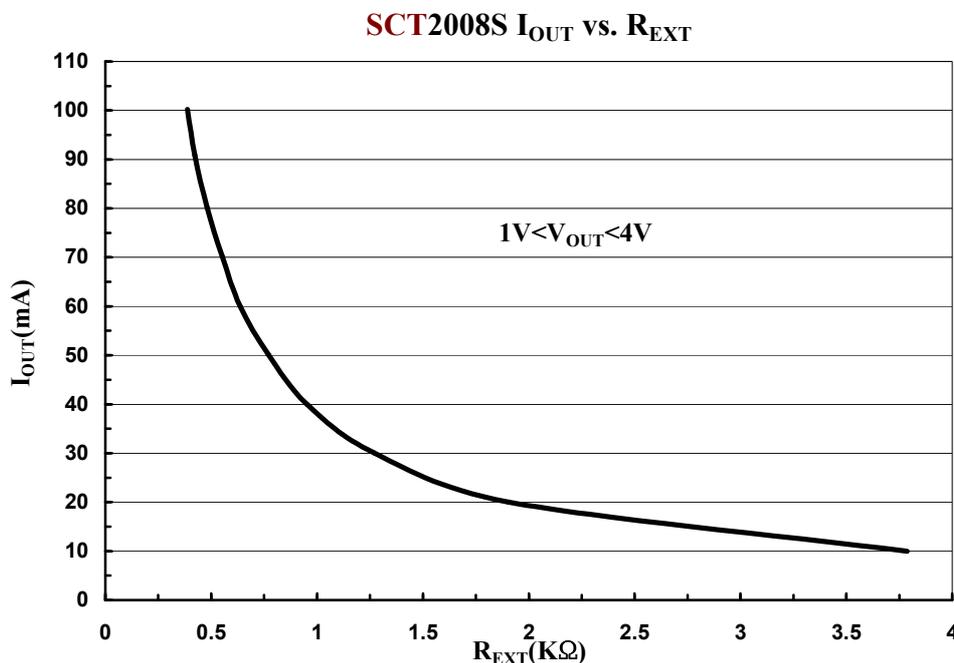| Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation delay time ("L" to "H")	OE - OUTn	t_{PLH}	$V_{DD} = 3.3/5V$ $V_{LED} = 5V$ $V_{IH} = V_{DD}$ $V_{IL} = GND$ $R_{EXT} = 900Ω$ $R_L = 90Ω$ $C_L = 10pF$ $C_1 = 1uF$ $C_{LED} = 10uF$	-	60	100	ns
Propagation delay time ("H" to "L")	OE - OUTn	t_{PHL}		-	60	100	ns
Pulse width	OE	t_w		200	-	-	ns
Output rise time of I_{OUT}		t_{OR}		-	80	100	ns
Output fall time of I_{OUT}		t_{OF}		-	60	100	ns

Test Circuit for Switching Characteristics
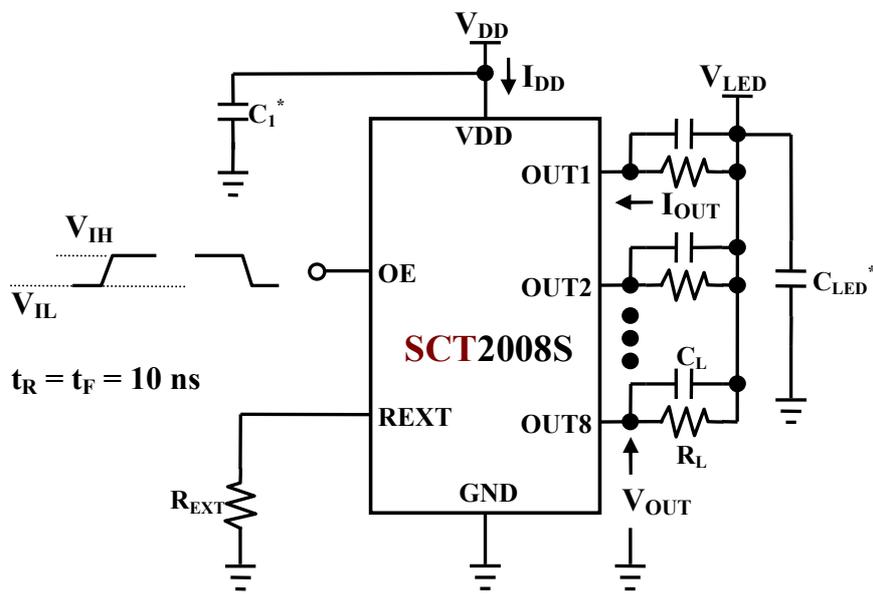
Place the C_1/C_{LED} more close to IC VDD/OUT pin(not power supply) as possible.
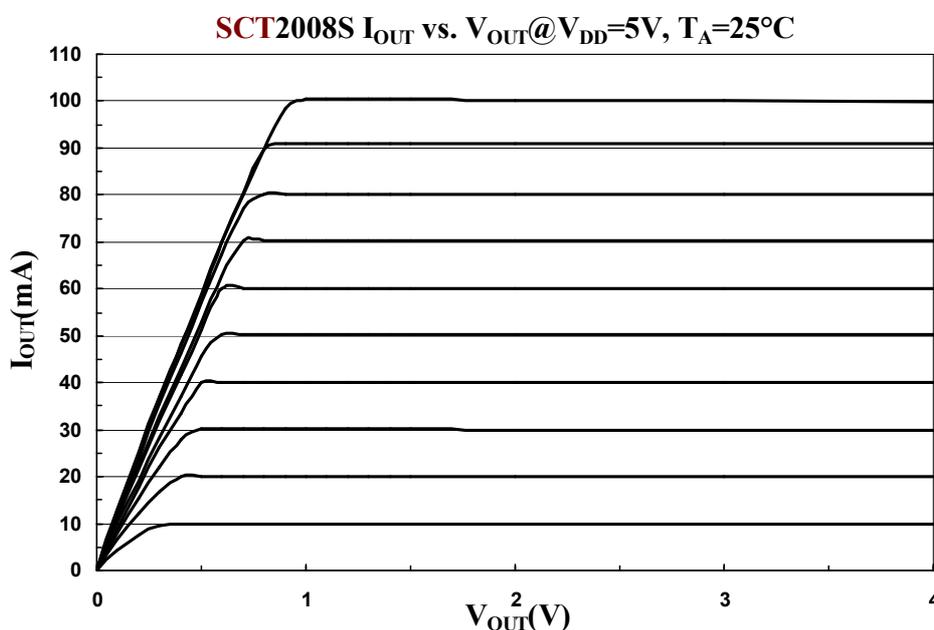
Timing Waveform
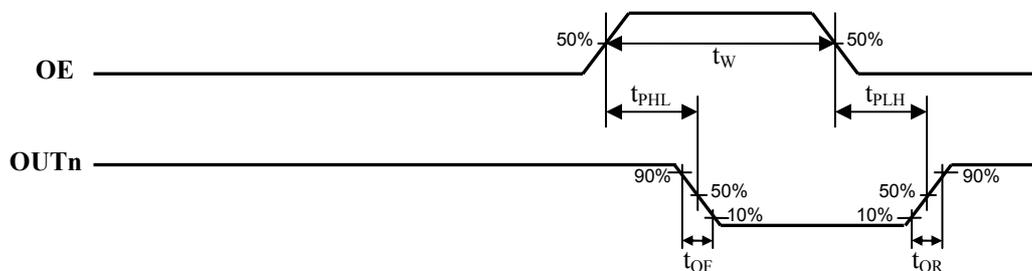
Adjusting Output Current

All SCT2008S's output current (I_{OUT}) are set by one external resistor at pin REXT. The output current I_{OUT} versus resistance of R_{EXT} is shown as the following figure.

SCT2008S I_{OUT} vs. R_{EXT}

$1V < V_{OUT} < 4V$

[Graph: I_{OUT}(mA) vs R_{EXT}(KΩ), curve decreasing from ~100mA at 0.4KΩ to ~10mA at 3.8KΩ]
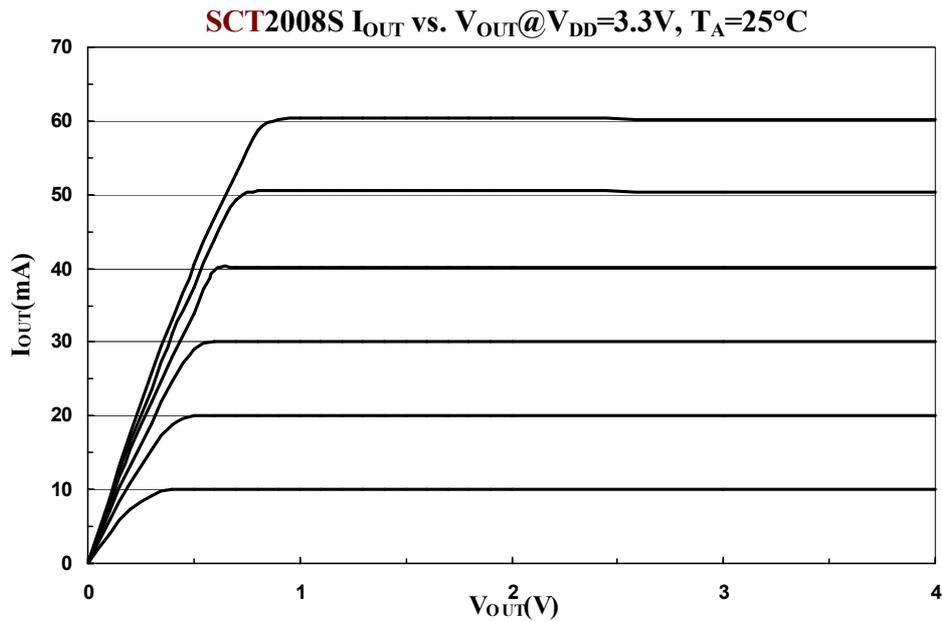
Furthermore, when the SCT2008S's output voltage is set between 1 Volt and 4 Volt, the output current can be estimated approximately by: $I_{OUT} = 60(630 / R_{EXT})$ (mA) (chip skew < ±6%). Thus the output current are set about 42mA at $R_{EXT} = 900Ω$.

Output Characteristics

The current characteristic of output curve is flat. The output current can kept constant regardless of the variations of LED forward voltage when $V_{OUT} > 1V$. The relationship between I_{OUT} and V_{OUT} is shown below:

SCT2008S I_{OUT} vs. V_{OUT}@V_{DD}=5V, T_A=25°C

[Graph: I_{OUT}(mA) vs V_{OUT}(V), multiple curves leveling off at various constant currents from 10mA to 100mA]

**SCT2008S I_{OUT} vs. V_{OUT}@V_{DD}=3.3V, T_A=25°C**

Two Steps Current Ramp

The SCT2008S provides two steps current ramp to lower the output switching noise, especially when LEDs are driven with larger sink current. The output waveform shown below is the SCT2008S connected under "Test Circuit for Switching Characteristics" and OE input with minimum PWM pulse width 200ns.
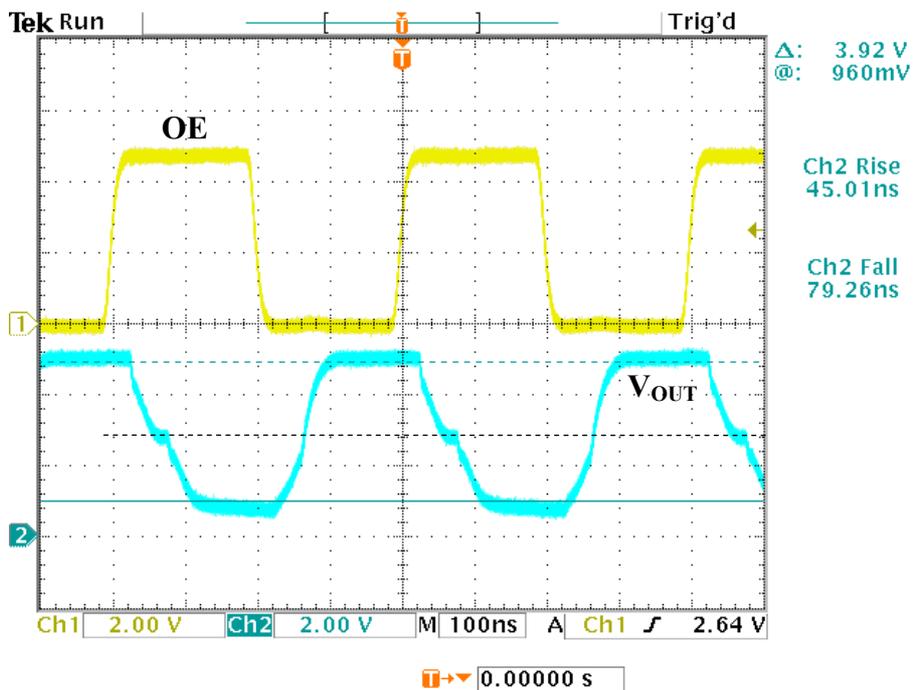
Maximum Power Dissipation

The maximum power dissipation ($P_{D(max)}$) of a semiconductor chip varies with different packages and ambient temperature. It's determined as $P_{D(max)}=(T_{J(max)}-T_A)/R_{TH(j-a)}$ where $T_{J(max)}$: maximum chip junction temperature is usually considered as 150°C, T_A: ambient temperature, $R_{TH(j-a)}$: thermal resistance. Since P=IV, for sinking larger I_{OUT}, users had better add proper voltage reducers on outputs to reduce the heat generated from the SCT2008S.


SCT2008S $P_{D(max)}$ vs. T_A
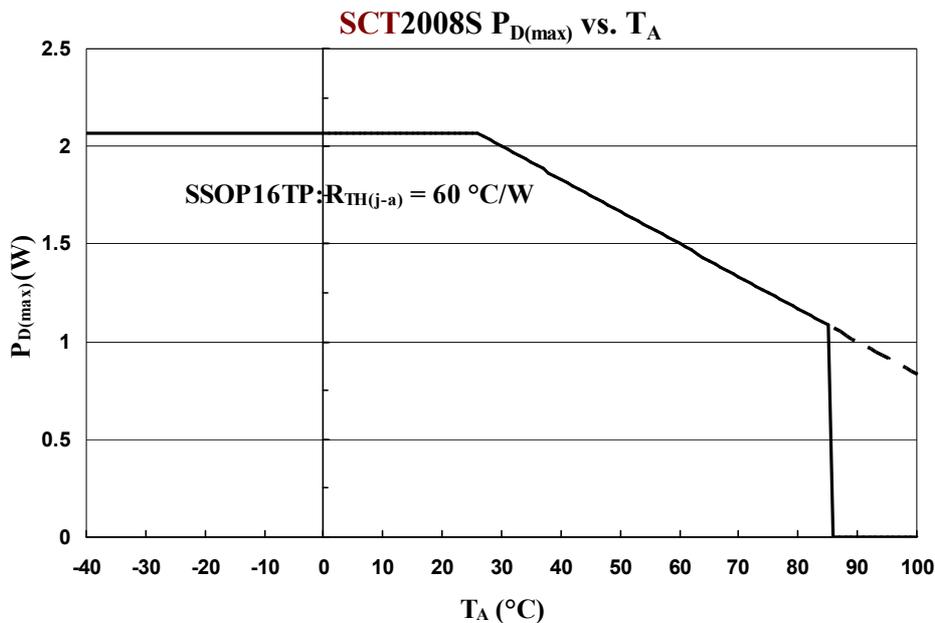
Limitation on Maximum Output Current

The maximum output current vs. duty cycle is estimated by:

$I_{OUT(max)}=(((T_{J(max)}-T_A)/R_{TH(j-a)})-(V_{DD}*I_{DD}))/V_{OUT}/Duty/N$, where $T_{J(max)}=150°C$, N=8(all ON)

SCT2008S $I_{OUT(max)}$ vs. Duty @SSOP16TP:60°C/W
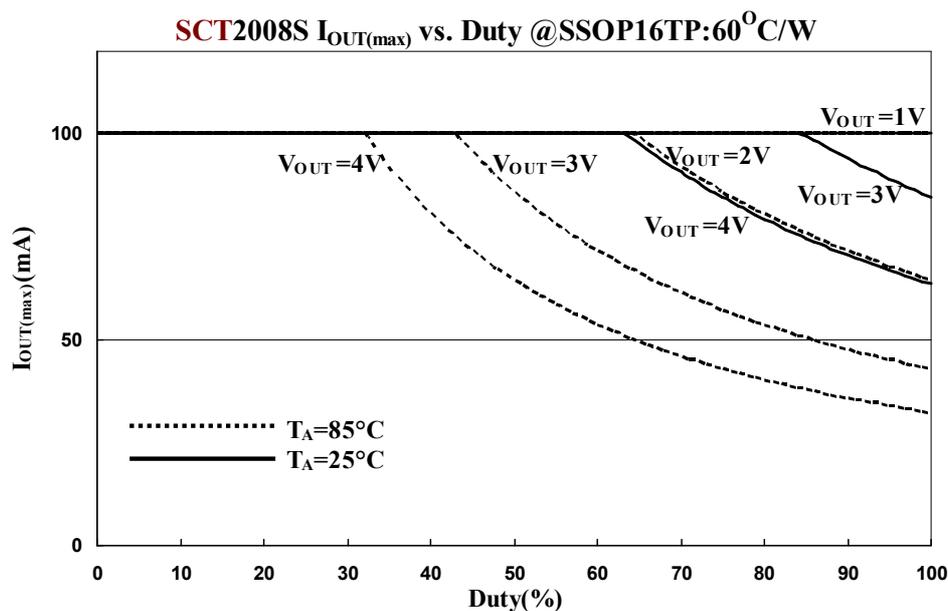
Load Supply Voltage (V$_{LED}$)

The SCT2008S can be operated very well when V_{OUT} ranges from 1V to 4V. It is recommended to use the lowest possible supply voltage or set a voltage reducer to reduce the V_{OUT} voltage, at the same time reduce the power dissipation of the SCT2008S. This can prevent the IC from malfunction with thermal situation. Follow the diagram instructions shown below to lower down the output voltage. This can be done by adding additional resistor or zener diode, thus $V_{OUT}=V_{LED}-V_{DROP}-V_F$.
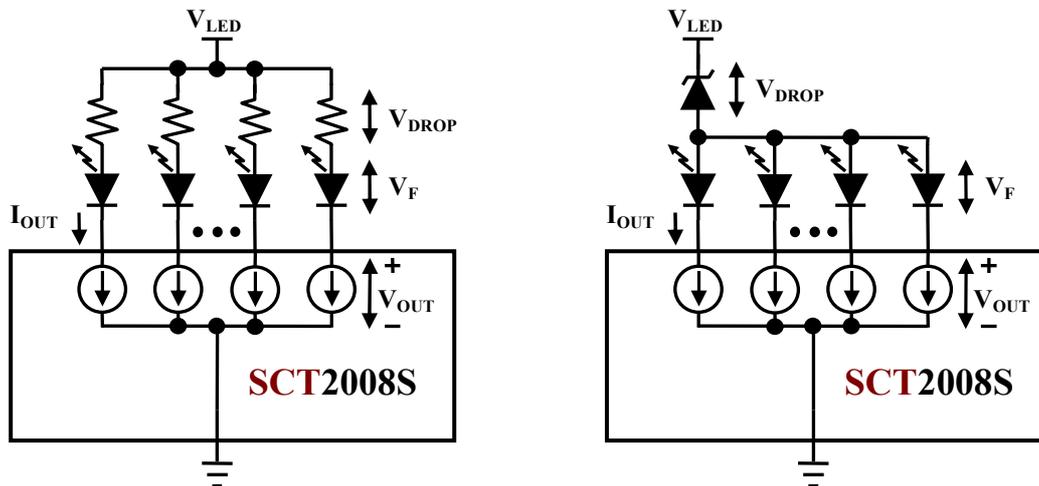

Over Temperature Shutdown

The SCT2008S contains thermal shutdown scheme to prevent damage from over-heating. The internal thermal sensor turns off all outputs when the die temperature exceeds +160°C. The outputs are enabled again when the die temperature drops below +110°C. During the thermal shutdown process, the LEDs look blinking since it is turned OFF then ON periodically.

Typical Application Circuits

(1) Lighting with recommended V_{LED}=3.3/5V
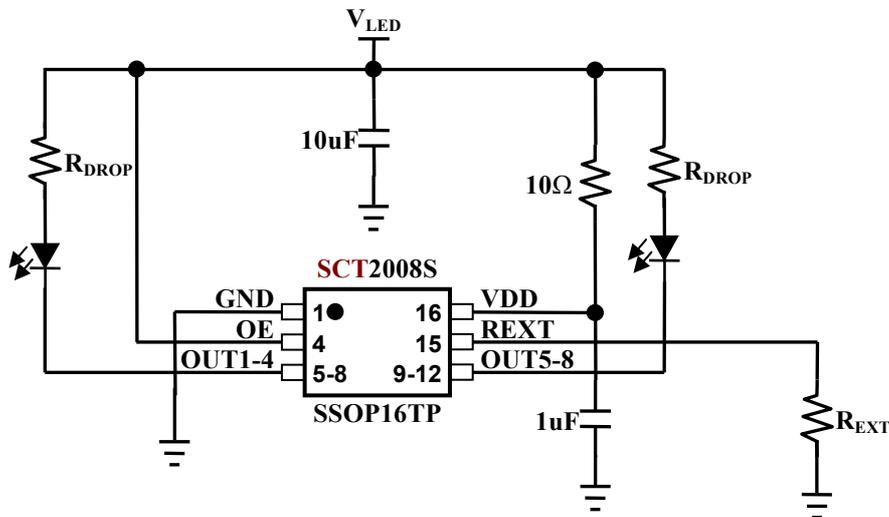
(2) Lighting with V_{LED} > 5V, e.g. V_{LED}=12V/24V

Components suggestion:

R_1=(V_{LED}-V_Z)/(I_{DD}+I_Z)

If V_{LED}=24V, V_Z=5.1V, I_Z=1mA

R_{EXT}=900Ω, $I_{DD(max)}$=10mA, then

R_1~1.7K is obtained. Beware that:
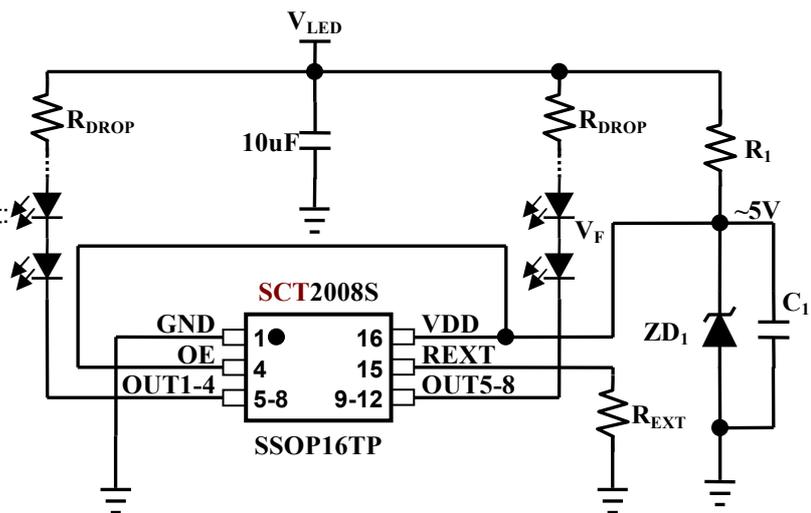
I_{DD} is R_{EXT} dependent, the higher

R_{EXT} the lower I_{DD}, vice versa.

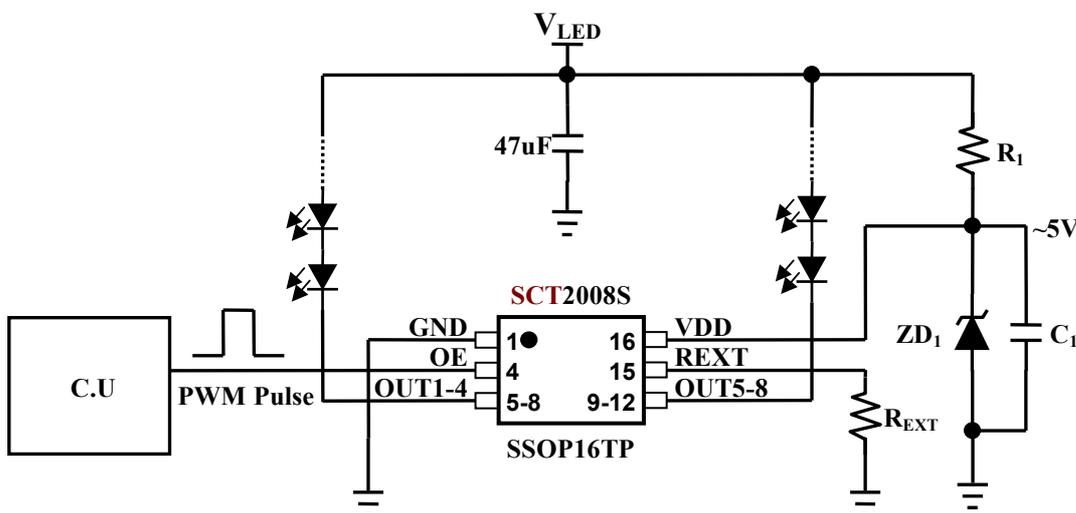R_{DROP}=(V_{LED}-n*V_F-V_{DO})/I_{OUT}

V_{DO} is the drop-out voltage of

intended output current.

C_1=1uF

(3) Lighting with dimming control

PCB Design Considerations

Use the following general guide-line when designing printed circuit boards (PCB) :

Decoupling Capacitor

Place a decoupling capacitor e.g. 1uF between VDD and GND pins of the SCT2008S. Locate the capacitor as close to the SCT2008S as possible. The necessary capacitance depends on the LED load current and dimming frequency. Inadequate VDD decoupling can cause timing problems, and very noisy LED supplies can affect LED current regulation.
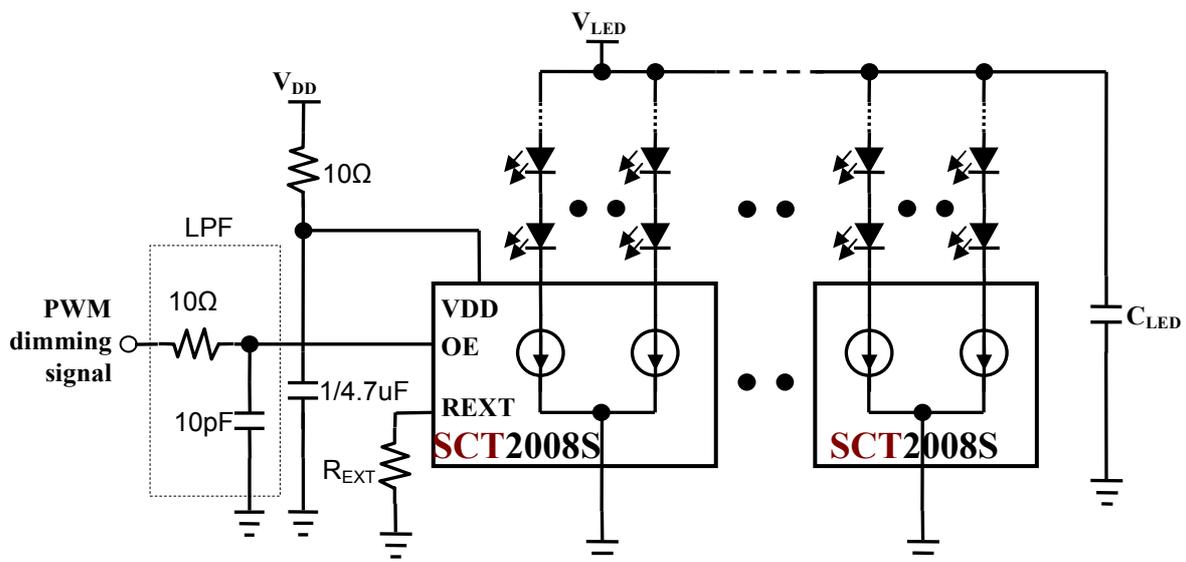
External Resistor (R$_{EXT}$)

Locate the external resistor as close to the REXT pin in as possible to avoid noise.

Power and Ground

Maximizing the width and minimizing the length of VDD and GND trace improves efficiency and ground bouncing by effect of reducing both power and ground parasitic resistance and inductance. A small value of resistor, e.g., 10Ω (higher if I$_{OUT}$ is larger) series in power input of the SCT2008S in conjunction with decoupling capacitor shunting the IC is recommended. Separating and feeding the LED power from another stable supply terminal V$_{LED}$, furthermore adding a capacitor C$_{LED}$ greater than 10uF beside the LED are recommended. Please adapt C$_{LED}$ according to total system current consumption.

EMI Reduction

To reduce the EMI radiation from system, an economical solution of RC low pass filter (LPF) is suggested to be used to lower the transient edge of PWM dimming signal OE, as shown in the figure above. Using at least four layers PCB board with two interior power and ground planes is a good scheme to decrease the signal current path which is the source of radiation emission. As a result, EMI radiation can be decreased.

Thermal Pad Consideration

The "thermal pad" (also named as "exposed pad") SSOP16 package beneath is NOT directly wired to ground terminal (pin1) internally. User should be aware of this electrical connection when designing the PCB board. In most application, connecting the thermal pad to system ground is strongly suggested.

In general, the heat generated from an IC is conducted to the PCB then radiates to the ambient. Thermal pad specifically increases the maximum power dissipation capability of the IC packages. To provide lower thermal resistance from the IC to the ambient air, PCB designers should layout larger thermal conduction areas on top layer (component side) and bottom layer as well as thermal vias, the more the better. In addition, connecting thermal via to the ground plane also increases thermal conduction areas, this improves the heat transfer efficiency at the same time greatly dissipates heat generated from the package. Furthermore, coating solder on bottom layer and selecting e.g. 2 oz. copper which will increase the total thickness of thermal conduction is an alternative.

When making the solder paste screen, an opening should be created for the thermal pad. This way the thermal pad can be electrically and thermally connected to the PCB. As the thermal pad is soldered on copper polygon, the chance of inadvertently shorting the thermal pad to traces routed underneath it could be eliminated.

Package Dimension

SSOP16TP(check up-to-date version)

Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.35	1.50	1.65	53.1	59.1	65.0
A1	0.00	-	0.10	0.0	-	3.9
A2	-	1.45	-	-	57.1	-
b	0.20	0.25	0.30	7.9	9.8	11.8
c	0.19	-	0.25	7.5	-	9.8
D	4.80	-	5.00	189.0	-	196.9
E	5.80	6.00	6.20	228.3	236.2	244.1
E1	3.80	3.90	4.00	149.6	153.5	157.5
D2	-	2.79	-	-	110.0	-
E2	-	2.54	-	-	100.0	-
e	-	0.64	-	-	25.2	-
L	0.40	-	1.27	15.7	-	50.0
y	-	-	0.10	-	-	3.9
θ	0°	-	8°	0°	-	8°

Revision History(check up-to-date version)

Data Sheet Version	Remark
V01_03	QFN package removed

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