Specification for Approval

Customer:_____

Model Name:_____

Supplier Approval			Customer approval
R&D Designed	R&D Approved	QC Approved	
Peter	Peng Jun		

Revision Record

REV NO.	REV DATE	CONTENTS	Note
A	2020-09-08	NEW ISSUE	

Table of Contents

1. Scope

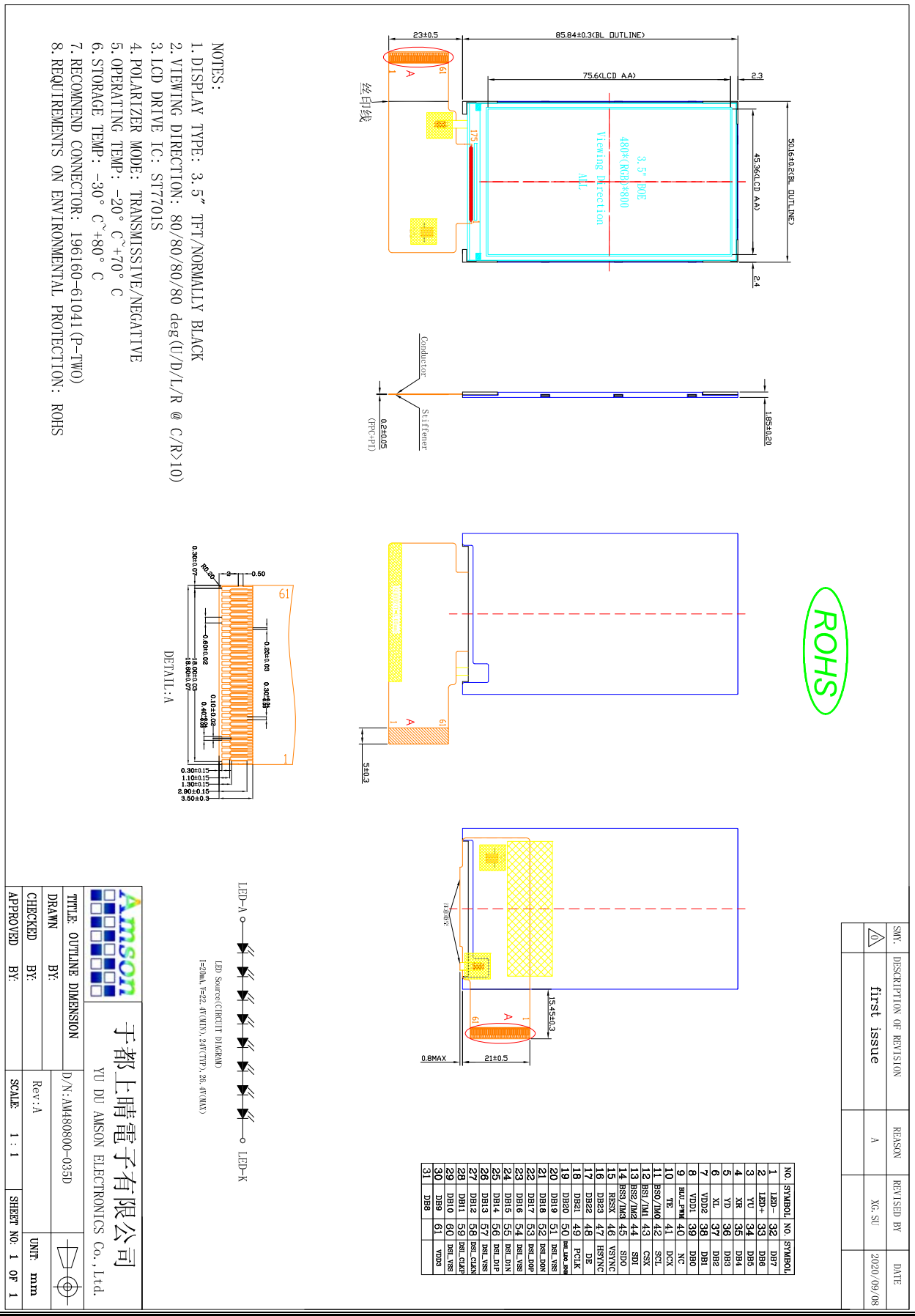
This specification defines general provisions as well as inspection standards for TFT module supplied by AMSON electronics.

If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution.

2. General Information

ITEM	STANDARD VALUES	UNITS
LCD type	3.5”TFT	--
Dot arrangement	480(RGB)×800	dots
Color filter array	RGB vertical stripe	--
Display mode	IPS / Transmission / Normally Black	-
Viewing Direction	80/80/80/80 deg(U/D/L/R @ C/R>10)	--
Driver IC	ST7701S	--
Module size	50.16(W)×85.84(H)×1.85(T)	mm
Active area	45.36(W)×75.60(H)	mm
Dot pitch	0.0945(W)×0.0945(H)	mm
Interface	3 SPI + 16-/18-/24-bit RGB interface 4 SPI + 16-/18-/24-bit RGB interface MIPI interface	--
Operating temperature	-20 ~ +70	°C
Storage temperature	-30 ~ +80	°C
Back Light	8 White LED	--

3. External Dimensions



NO.	SYMBOL	NO.	SYMBOL
1	LED-	32	DB7
2	LED+	33	DB6
3	YU	34	DB5
4	XR	35	DB4
5	YD	36	DB3
6	XL	37	DB2
7	VDD2	38	DB1
8	VDD1	39	DB0
9	BLU_PWM	40	NC
10	TE	41	DCX
11	BS0/IM0	42	SCL
12	BS1/IM1	43	CSX
13	BS2/IM2	44	SDI
14	BS3/IM3	45	SDO
15	RESX	46	VSYNC
16	DB23	47	HSYNC
17	DB22	48	DE
18	DB21	49	PCLK
19	DB20	50	DGL_LOG_DATA
20	DB19	51	DSL_VSS
21	DB18	52	DSL_DON
22	DB17	53	DSL_DOP
23	DB16	54	DSL_VSS
24	DB15	55	DSL_DIN
25	DB14	56	DSL_DIP
26	DB13	57	DSL_VSS
27	DB12	58	DSL_CLKN
28	DB11	59	DSL_CLKP
29	DB10	60	DSL_VSS
30	DB9	61	VDD3
31	DB8		

4. Interface Description

PIN	PIN NAME	DESCRIPTION
1	LEDK	LED backlight (Cathode).
2	LEDA	LED backlight (Anode).
3	NC(YU)	NC(Touch PIN)
4	NC(XR)	
5	NC(YD)	
6	NC(XL)	
7	VDD2	A supply voltage to the analog circuit.
8	VDD1	A supply voltage to the I/O circuit.
9	BLU_PWM	The PWM frequency output for LCD driver control. ***Leave the pin open when not in use.***
10	TE	Output a frame head pulse signal.
11	BS0/IM0	MPU interface mode selection signal. Must be connected to GND or VDD1.For the details, please refer to NOTE3.
12	BS1/IM1	
13	BS2/IM2	
14	BS3/IM3	
15	RESX	Reset input pin, Active “L”.
16~39	DB[23:00]	Data bus. For the connection condition of the RGB Interface mode, please refer to NOTE3 ***Fix to VDDI or DGND level when not in use.***
40	NC	NC
41	DCX	- The SPI interface (DCX): The signal for command or parameter select. Low: Command High: Parameter ***Fix to VDDI or DGND level when not in use.***
42	SCL	SCL: Serial clock input for SPI interface. ***Fix to VDDI or DGND level when not in use.***
43	CSX	- A chip select signal Low: the chip is selected and accessible High: the chip is not selected and not accessible ***Fix to VDDI or DGND level when not in use.***
44	SDI	SDA: Serial data input/output bidirectional pin for SPI Interface. ***Fix to DGND level when not in use.***
45	SDO	Serial data output pin used for the SPI Interface. ***Leave the pin open when not in use.***
46	VSYNC	Frame synchronizing signal for RGB interface operation ***Fix to VDDI or DGND level when not in use.***
47	HSYNC	Line synchronizing signal for RGB interface operation ***Fix to VDDI or DGND level when not in use.***
48	DE	Data enable signal for RGB interface operation Low: access enabled High: access inhibited ***Fix to VDDI or DGND level when not in use.***

49	PCLK	Dot clock signal for RGB interface operation ***Fix to VDDI or DGND level when not in use.***
50	DSI_LDO_ENB	**NC**
51	DSI_VSS	Ground.
52	DSI_D0N	MIPI-DSI Data differential signal input pins. (Data lane 0)
53	DSI_D0P	MIPI-DSI Data differential signal input pins. (Data lane 0)
54	DSI_VSS	Ground.
55	DSI_D1N	MIPI-DSI Data differential signal input pins. (Data lane 1)
56	DSI_D1P	MIPI-DSI Data differential signal input pins. (Data lane 1)
57	DSI_VSS	Ground.
58	DSI_CLKN	MIPI-DSI CLOCK differential signal input pins.
59	DSI_CLKP	MIPI-DSI CLOCK differential signal input pins.
60	DSI_VSS	Ground.
61	VDD3	A supply voltage to the logic circuit.

NOTE3:

IM3	IM2	IM1	IM0	Interface Mode	DB pins
0	0	0	1	SPI 4wire+RGB 16BIT /FALL	(DB0-DB4)=(B0-B4),(DB8-DB13)=(G0-G5),(DB16-DB20)=(R0-R4)
				SPI 4wire+RGB 18BIT /FALL	(DB0-DB5)=(B0-B5),(DB6-DB11)=(G0-G5),(DB12-DB17)=(R0-R5)
				SPI 4wire+RGB 24BIT /FALL	(DB0-DB7)=(B0-B7),(DB8-DB15)=(G0-G7),(DB16-DB23)=(R0-R7)
0	0	1	0	SPI 3wire+RGB 16BIT /FALL	(DB0-DB4)=(B0-B4),(DB8-DB13)=(G0-G5),(DB16-DB20)=(R0-R4)
				SPI 3wire+RGB 18BIT /FALL	(DB0-DB5)=(B0-B5),(DB6-DB11)=(G0-G5),(DB12-DB17)=(R0-R5)
				SPI 3wire+RGB 24BIT /FALL	(DB0-DB7)=(B0-B7),(DB08-DB15)=(G0-G7),(DB16-DB23)=(R0-R7)
0/1	1	0	1	MIPI	DSI_D0N,DSI_D0P,DSI_D1N,DSI_D1P,DSI_CLKN,DSI_CLKP
1	0	0	1	SPI 4wire+RGB 16BIT /RISE	(DB0-DB4)=(B0-B4),(DB8-DB13)=(G0-G5),(DB16-DB20)=(R0-R4)
				SPI 4wire+RGB 18BIT /RISE	(DB0-DB5)=(B0-B5),(DB6-DB11)=(G0-G5),(DB12-DB17)=(R0-R5)
				SPI 4wire+RGB 24BIT /RISE	(DB0-DB7)=(B0-B7),(DB8-DB15)=(G0-G7),(DB16-DB23)=(R0-R7)
1	0	1	0	SPI 3wire+RGB 16BIT /RISE	(DB0-DB4)=(B0-B4),(DB8-DB13)=(G0-G5),(DB16-DB20)=(R0-R4)
				SPI 3wire+RGB 18BIT /RISE	(DB0-DB5)=(B0-B5),(DB6-DB11)=(G0-G5),(DB12-DB17)=(R0-R5)
				SPI 3wire+RGB 24BIT /RISE	(DB0-DB7)=(B0-B7),(DB8-DB15)=(G0-G7),(DB16-DB23)=(R0-R7)

5. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Logic Supply Voltage	VDD1	-0.3	4.6	V
Analog Supply Voltage	VDD2,3	-0.3	4.6	V
Input Voltage	Vin	-0.3	VDD1+0.3	V
Operating Temperature	TOP	-20	70	°C
Storage Temperature	TST	-30	80	°C
Storage Humidity	HD	20	90	%RH

6. DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Logic Supply Voltage	VDD1	1.65	1.8	3.3	V	-
Analog Supply Voltage	VDD2,3	2.5	2.8	3.6	V	-
Input High Voltage	V_{IH}	0.7VDD1	-	VDD1	V	-
Input Low Voltage	V_{IL}	GND	-	0.3VDD1	V	-
Output High Voltage	V_{OH}	0.8VDD1	-	VDD1	V	IOH = -1.0mA
Output Low Voltage	V_{OL}	GND	-	0.2VDD1	V	-
I/O Leak Current	I_{LI}	-1	-	1	uA	-

7. Timing Characteristics
7.1 Reset Timing Characteristics

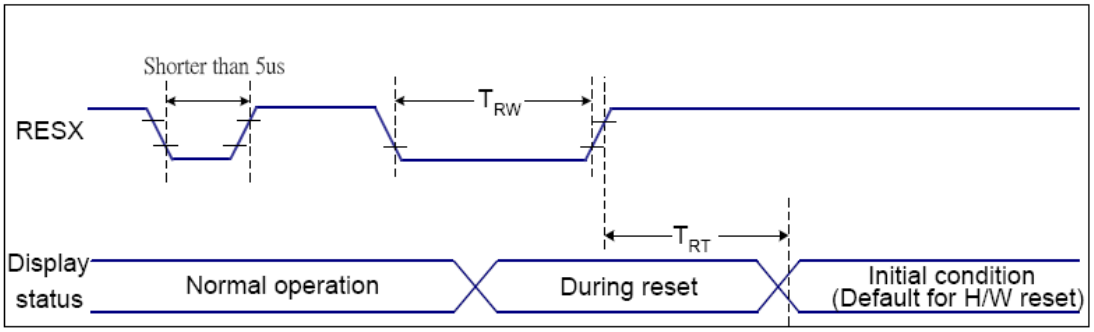


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

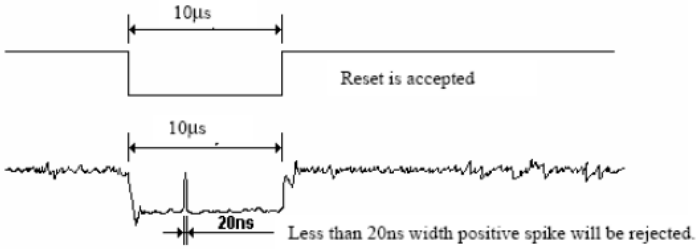
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



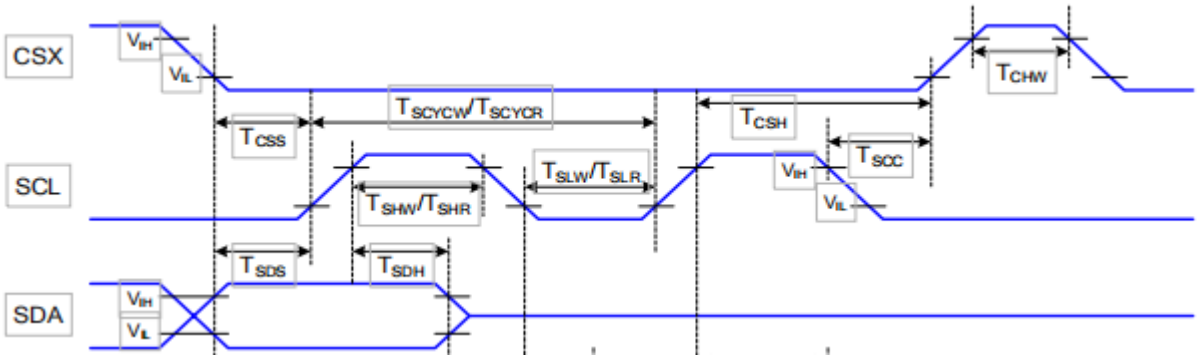
5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

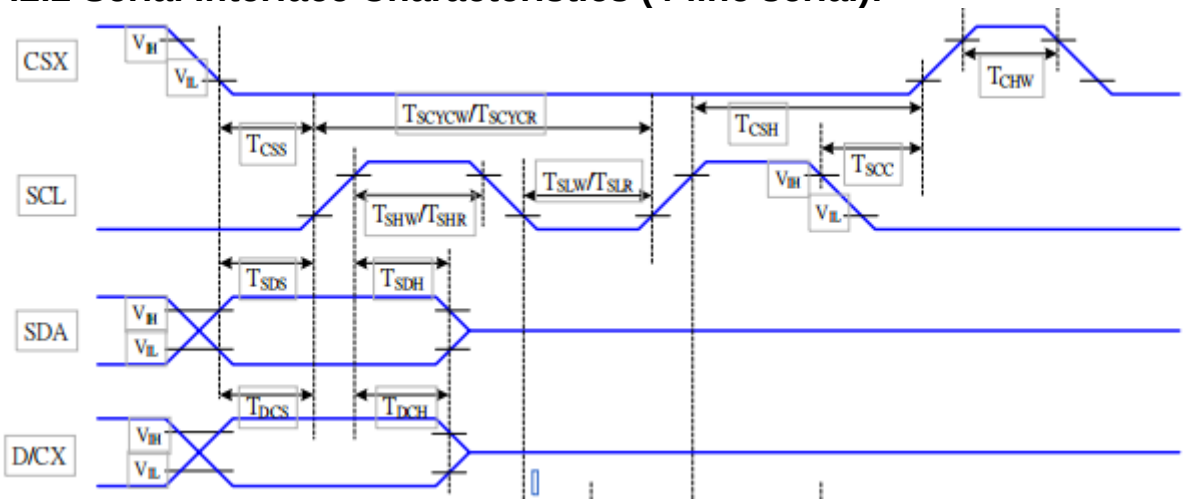
7.2 AC Characteristics

7.2.1 Serial Interface Characteristics (3-line serial):



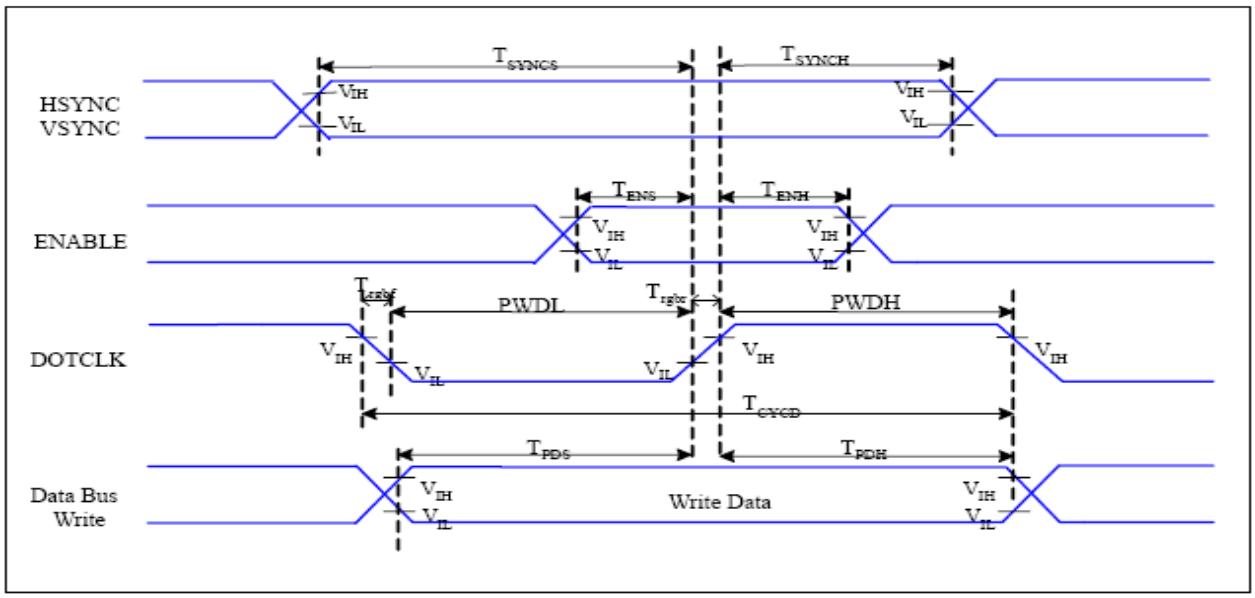
Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	60		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

7.2.2 Serial Interface Characteristics (4-line serial):



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

7.2.3 RGB Interface Characteristics



VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

Table 6 18/16 Bits RGB Interface Timing Characteristics

7.3 MIPI Interface Characteristics:

7.3.1 High Speed Mode

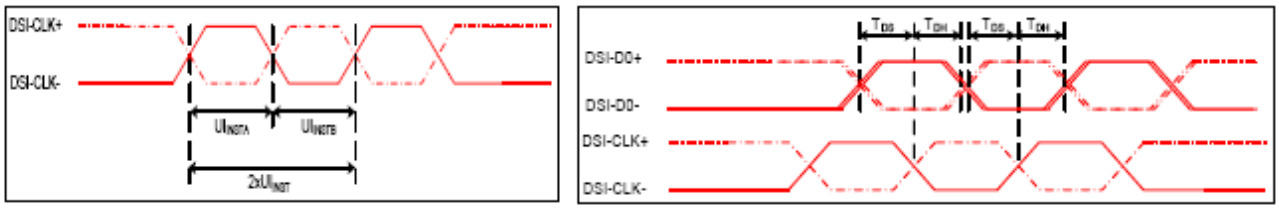


Figure 4 DSI clock channel timing

Figure 5 Rising and falling time on clock and data channel

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

7.3.2 Lowe Power Mode

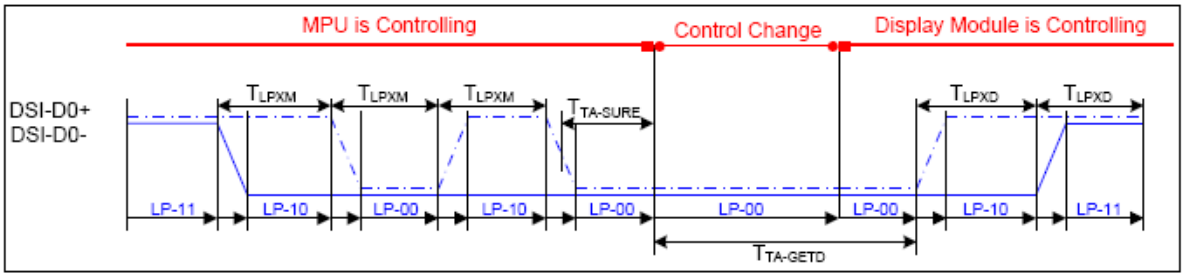


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

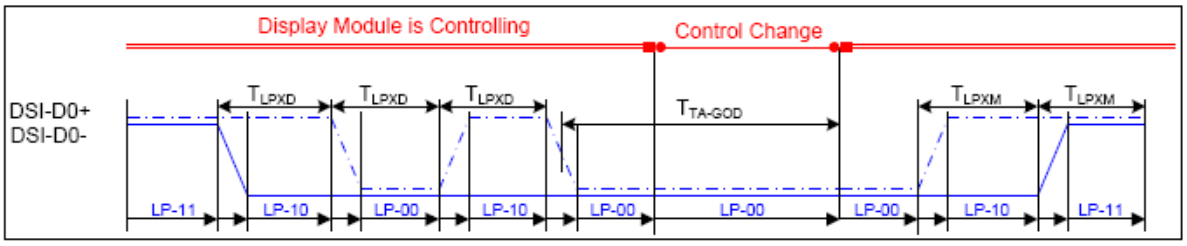


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

Table 8 Mipi Interface Low Power Mode Timing Characteristics

7.3. 3DSI Bursts Mode

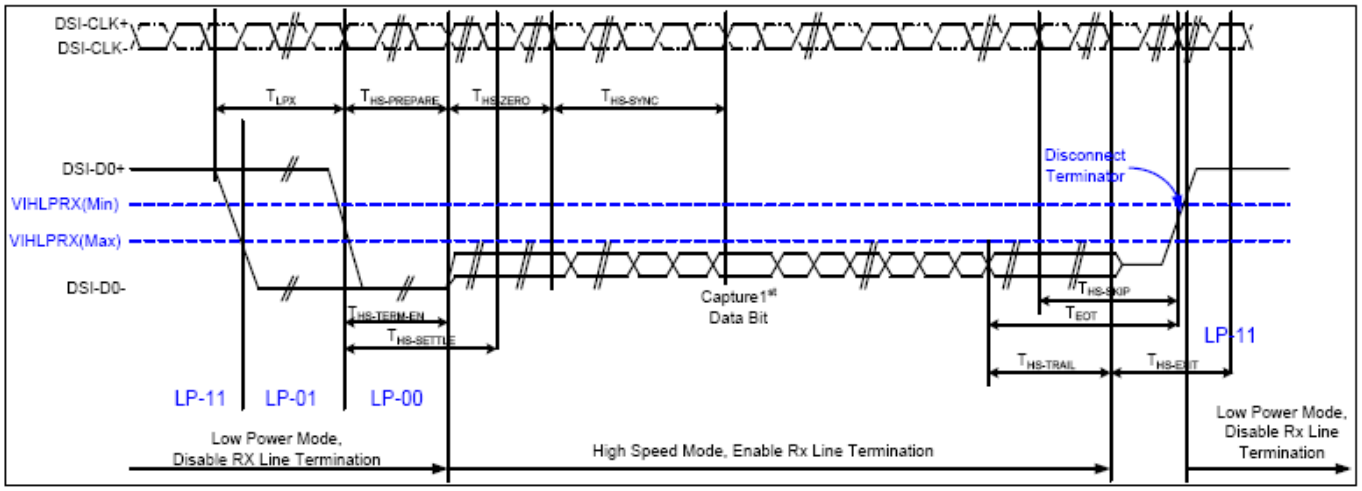


Figure 7 Data lanes-Low Power Mode to/from High Speed Mode Timing

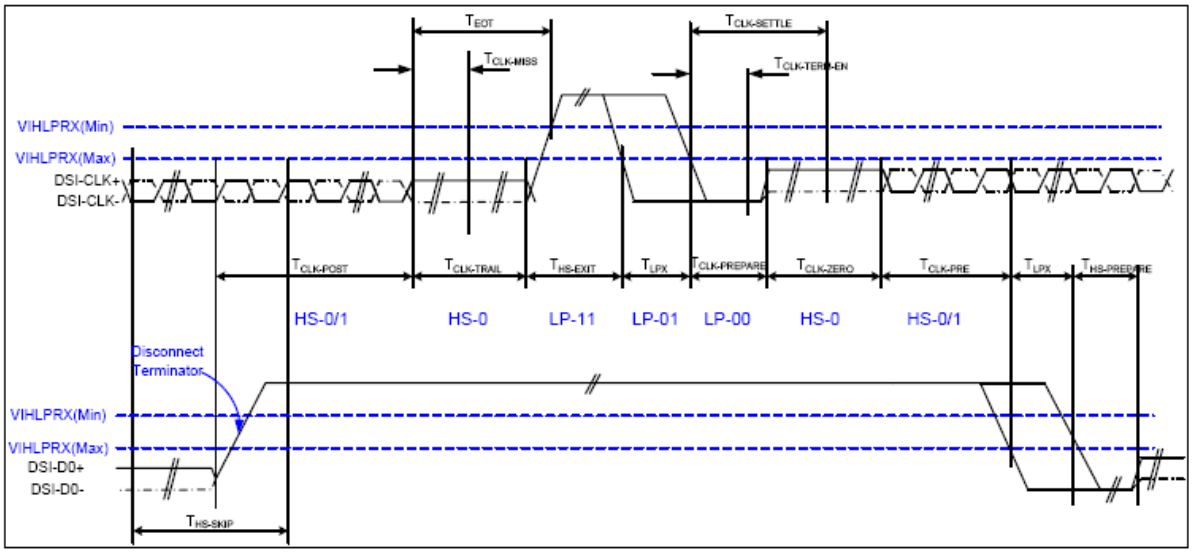


Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

8. Backlight Characteristics

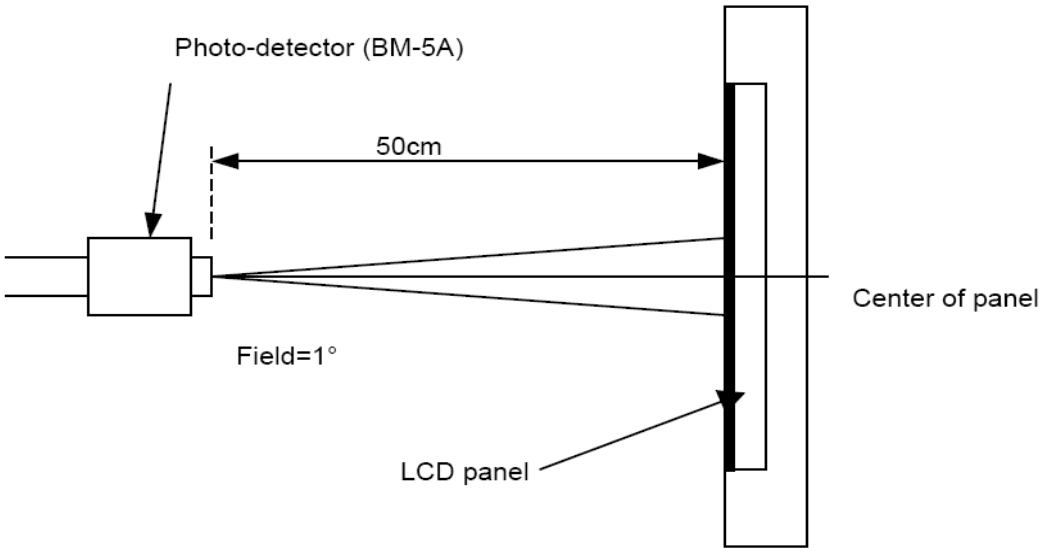
LED CIRCUIT:

Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition
Supply Voltage	Vf	22.4	24	26.4	V	If=20mA
Supply Current	If	-	20	-	mA	-
Luminous Intensity for LCM	-	350	400	-	cd/m^2	If=20mA
Uniformity for LCM	-	80	-	-	%	If=20mA
Life Time	-	-	50000	-	Hr	If=20mA
Backlight Color	White					

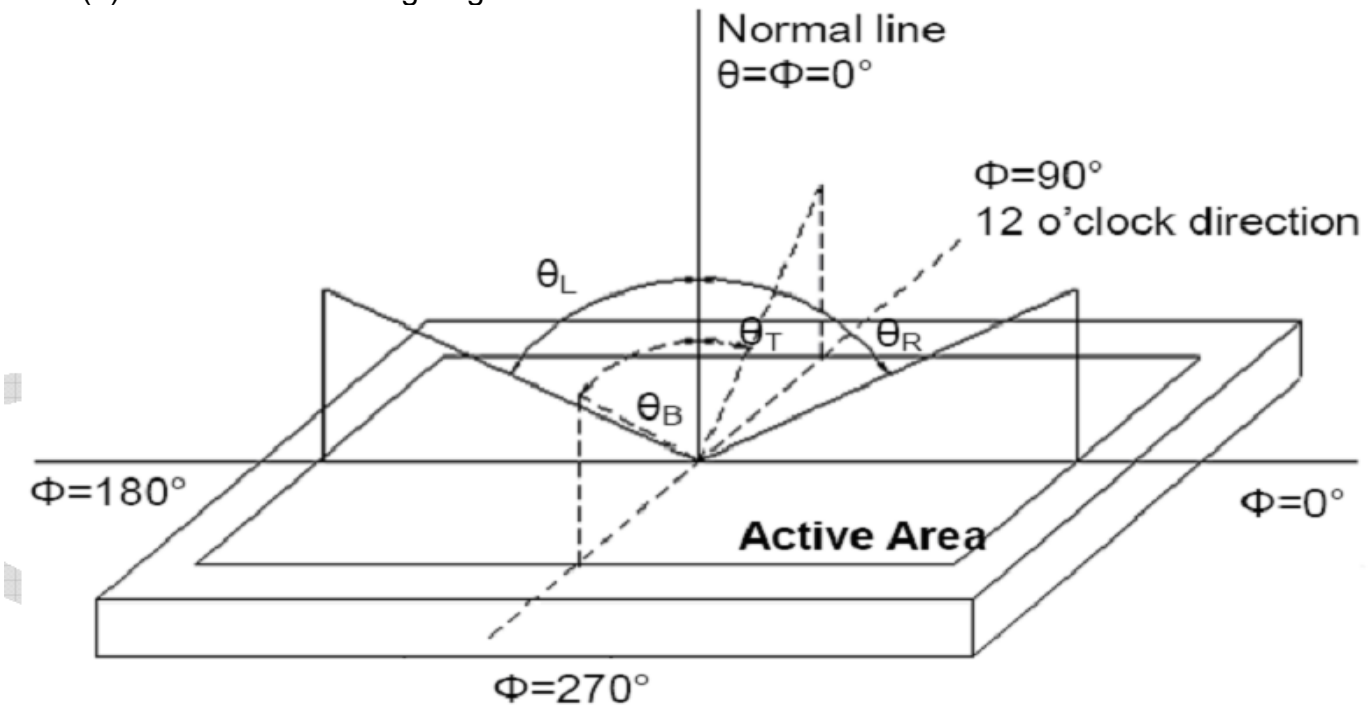
9. Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR>10)	Horizontal	θ_L	80	85	-	degree	(1),(2),(6)
		θ_R	80	85	-		
	Vertical	θ_T	80	85	-		
		θ_B	80	85	-		
Contrast Ratio	Center		800	1000	-	-	(1),(3),(6)
Response Time	Rising + Falling		-	-	35	ms	(1),(4),(6)
CF Color Chromaticity (CIE1931)	Red x		Typ. -0.05	0.66	Typ. +0.05	-	(1), (6)
	Red y			0.327		-	
	Green x			0.302		-	
	Green y			0.591		-	
	Blue x			0.138		-	
	Blue y			0.104		-	

Note (1) Measurement Setup: The LCD module should be stabilized at given temp. 25°C for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



Note (2) Definition of Viewing Angle



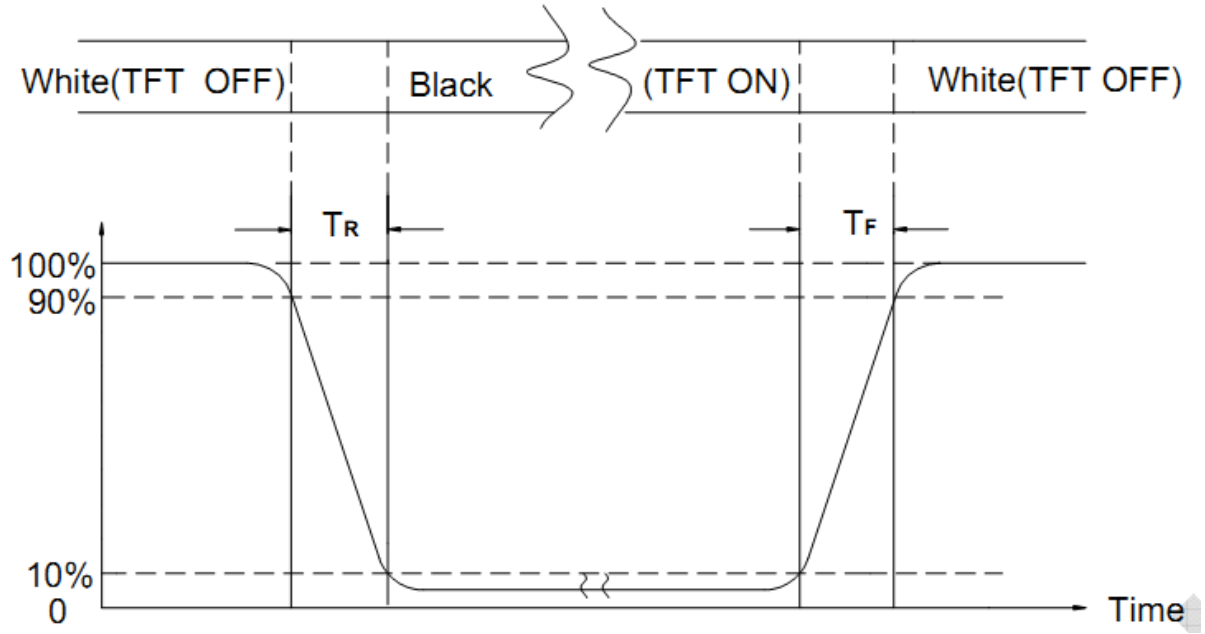
Note (3) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (4) Definition of response time



Note (5) Definition of Transmittance (Module is without signal input)

Transmittance = Center Luminance of LCD / Center Luminance of Back Light x 100%

Note (6) Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD

10. Reliability Test Conditions and Methods

NO.	TEST ITEMS	TEST CONDITION	INSPECTION AFTER TEST
□	High Temperature Storage	80°C±2°C×96Hours	Inspection after 2~4hours storage at room temperature, the samples should be free from defects: 1, Air bubble in the LCD. 2, Seal leak. 3, Non-display. 4, Missing segments. 5, Glass crack. 6, Current IDD is twice higher than initial value. 7, The surface shall be free from damage. 8, The electric characteristic requirements shall be satisfied.
□	Low Temperature Storage	-30°C±2°C×96Hours	
□	High Temperature Operating	70°C±2°C×96Hours	
□	Low Temperature Operating	-20°C±2°C×96Hours	
□	Temperature Cycle(Storage)	-20°C ⟺ 25°C ⟺ 70°C (30min) (5min) (30min) 1cycle Total 10cycle	
□	Damp Proof Test (Storage)	50°C±5°C×90%RH×96Hours	
□	Vibration Test	Frequency:10Hz~55Hz~10Hz Amplitude:1.5M X,Y,Z direction for total 3hours (packing condition test will be tested by a carton)	
□	Drooping Test	Drop to the ground from 1M height one time every side of carton. (packing condition test will be tested by a carton)	
□	ESD Test	Voltage:±8KV,R:330Ω,C:150PF,Air Mode,10times	

REMARK:
1, The Test samples should be applied to only one test item.
2, Sample side for each test item is 5~10pcs.
3,For Damp Proof Test, Pure water(Resistance＞10MΩ)should be used.
4,In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

11. Inspection Standard

11.1. QUALITY :

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

11.1.1. THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM AMSON TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10℃ TO 40℃ ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

11.1.2. INCOMING INSPECTION

(A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION , A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

(B) THE STANDARD OF QUALITY

ISO-2859-1 (SAME AS MIL-STD-105E) , LEVEL Ⅱ SINGLE PLAN.

CLASS	AQL(%)
CRITICAL	0.4 %
MAJOR	0.65 %
MINOR	1.5 %
TOTAL	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

(C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION , A LOT OUT IS DISCOVERED. PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

11.1.3. WARRANTY POLICY

AMSON WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. AMSON WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF AMSON.

11.2. CHECKING CONDITION

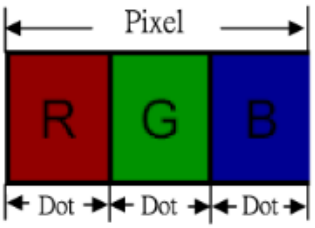
11.2.1.CHECKING DIRECTION SHALL BE IN THE 45 DEGREE AREA TO FACE THE SAMPLE.

11.2.2.CHECKER SHALL SEE OVER 300±25 mm. WITH BARE EYES FAR FROM SAMPLE AND USING 2 PCS. OF 20W FLUORESCENT LAMP.

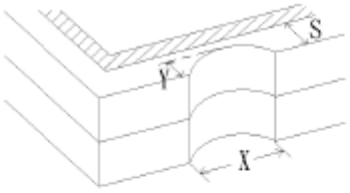
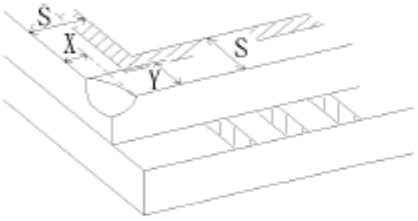
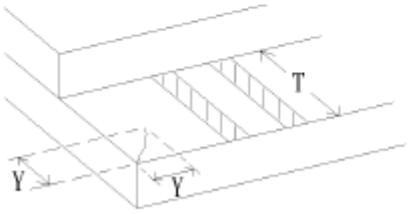
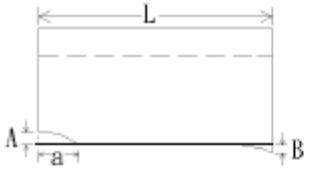
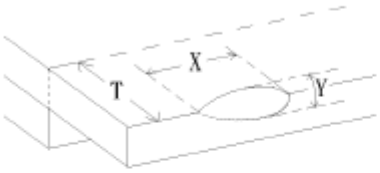
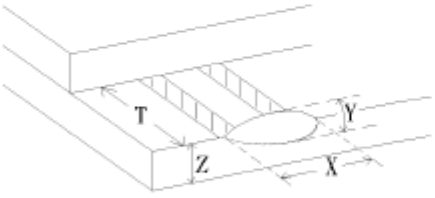
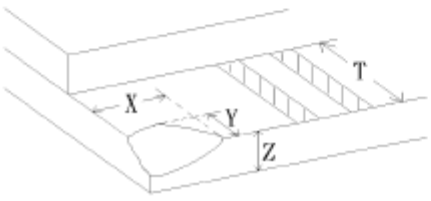
11.3. INSPECTION PLAN :

CLASS	ITEM	JUDGEMENT	CLASS
PACKING & INDICATE	1. OUTSIDE AND INSIDE PACKAGE	"MODEL NO." , "LOT NO." AND "QUANTITY" SHOULD INDICATE ON THE PACKAGE.	Minor
	2. MODEL MIXED AND QUANTITY	OTHER MODEL MIXED.....REJECTED QUANTITY SHORT OR OVER.....REJECTED	Critical
	3. PRODUCT INDICATION	"MODEL NO." SHOULD INDICATE ON THE PRODUCT	Major
ASSEMBLY	4. DIMENSION, LCD GLASS SCRATCH AND SCRIBE DEFECT.	ACCORDING TO SPECIFICATION OR DRAWING.	Major
APPEARANCE	5. VIEWING AREA	POLARIZER EDGE OR LCD'S SEALING LINE IS VISABLE IN THE VIEWING AREA .....REJECTED	Minor
	6. BLEMISH、BLACK SPOT、 WHITE SPOT IN THE LCD AND LCD GLASS CRACKS	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	7. BLEMISH、BLACK SPOT WHITE SPOT AND SCRATCH ON THE POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	8. BUBBLE IN POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION(INSIDE VIEWING AREA)	Minor
	9. LCD'S RAINBOW COLOR	STRONG DEVIATION COLOR (OR NEWTON RING) OF LCD.....REJECTED. OR ACCORDING TO LIMITED SAMPLE (IF NEEDED, AND INSIDE VIEWING AREA)	Minor
ELECTRICAL	10. ELECTRICAL AND OPTICAL CHARACTERISTICS (CONTRAST、VOP、 CHROMATICITY ... ETC)	ACCORDING TO SPECIFICATION OR DRAWING . (INSIDE VIEWING AREA)	Critical
	11.MISSING LINE	MISSING DOT、LINE、CHARACTER ....REJECTED	Critical
	12.SHORT CIRCUIT、 WRONG PATTERN DISPLAY	NO DISPLAY、WRONG PATTERN DISPLAY、CURRENT CONSUMPTION OUT OF SPECIFICATION..... REJECTED	Critical
	13. DOT DEFECT (FOR COLOR AND TFT)	ACCORDING TO STANDARD OF VISUAL INSPECTION	Minor

11.4. STANDARD OF VISUAL INSPECTION

<table>
<tr><th>NO.</th><th>CLASS</th><th>ITEM</th><th>JUDGEMENT</th></tr>
<tr><td>11.4.1</td><td>MINOR</td><td>BLACK AND WHITE SPOT
FOREIGN MATERIEL
DUST IN THE CELL
BLEMISH
SCRATCH</td><td>(A) ROUND TYPE: unit : mm.
<table>
<tr><th>DIAMETER (mm.)</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦ 0.1</td><td>DISREGARD</td></tr>
<tr><td>0.1 < Φ ≦ 0.25</td><td>3 (Distance>5mm)</td></tr>
<tr><td>0.25 < Φ</td><td>0</td></tr>
</table>
NOTE: Φ=(LENGTH+WIDTH)/2
(B) LINEAR TYPE: unit : mm.
<table>
<tr><th>LENGTH</th><th>WIDTH</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>------</td><td>W ≦0.03</td><td>DISREGARD</td></tr>
<tr><td>L ≦ 5.0</td><td>0.03 < W ≦0.07</td><td>3 (Distance>5mm)</td></tr>
<tr><td>------</td><td>0.07 < W</td><td>FOLLOW ROUND TYPE</td></tr>
</table></td></tr>
<tr><td>11.4.2</td><td>MINOR</td><td>BUBBLE IN POLARIZER
DENT ON POLARIZER</td><td>unit : mm.
<table>
<tr><th>DIAMETER</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦ 0.2</td><td>DISREGARD</td></tr>
<tr><td>0.2 < Φ ≦ 0.5</td><td>2 (Distance>5mm)</td></tr>
<tr><td>0.5 < Φ</td><td>0</td></tr>
</table></td></tr>
<tr><td>11.4.3</td><td>MINOR</td><td>Dot Defect</td><td>
<table>
<tr><th>Items</th><th>ACC. Q'TY</th></tr>
<tr><td>Bright dot</td><td>N≦ 4</td></tr>
<tr><td>Dark dot</td><td>N≦ 4</td></tr>
</table>
Pixel Define :
 

Note 1: The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.
Note 2: Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
Note 3: Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green ,blue pattern.</td></tr>
</table>

NO.	CLASS	ITEM	JUDGEMENT
11.4.4	MINOR	LCD GLASS CHIPPING	 Y > S Reject
11.4.5	MINOR	LCD GLASS CHIPPING	 X or Y > S Reject
11.4.6	MAJOR	LCD GLASS GLASS CRACK	 Y > (1/2) T Reject
11.4.7	MAJOR	LCD GLASS SCRIBE DEFECT	 1. a> L/3 , A>1.5mm. Reject 2. B : ACCORDING TO DIMENSION
11.4.8	MINOR	LCD GLASS CHIPPING (ON THE TERMINAL AREA)	 Φ= (x+y)/2 > 2.5 mm Reject
11.4.9	MINOR	LCD GLASS CHIPPING (ON THE TERMINAL SURFACE)	 Y > (1/3) T Reject
11.4.10	MINOR	LCD GLASS CHIPPING	 Y > T Reject

12. Handling Precautions

12.1 Mounting method

The LCD panel of AMSON TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

12.2 Caution of LCD handling and cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (Cl), Sulfur (S) from customer, Responsibility is on customer.

12.3 Caution against static charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to power or ground, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

12.4 packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the maximum operating temperature, 50%Rh or less is required.

12.6 storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.
  [It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

13. Precaution for Use

13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification.
- When a new problem is arisen this is not specified in this specification.
- When an inspection specifications change or operating condition change in customer is reported to AMSON TFT and some problem is arisen in this specification due to the change.
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.

14. Packing Method

TBD